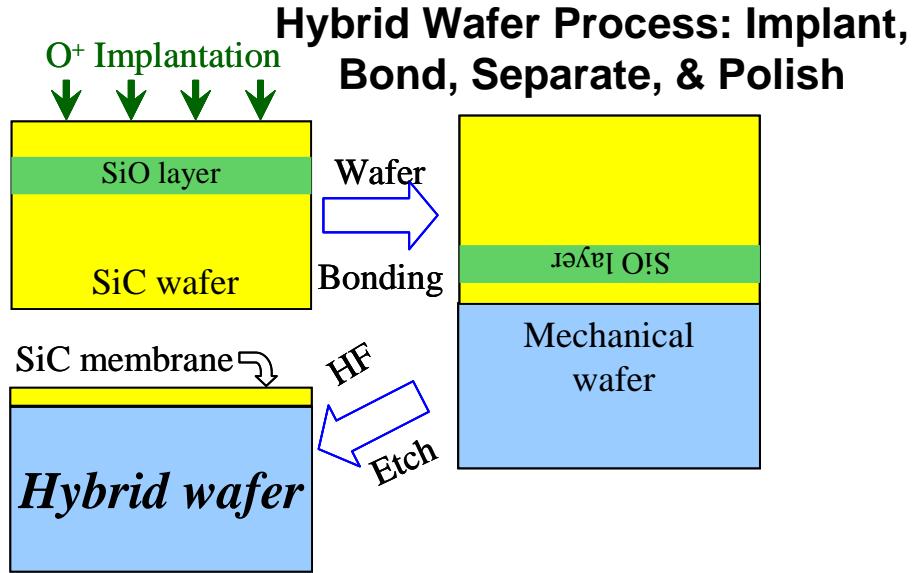
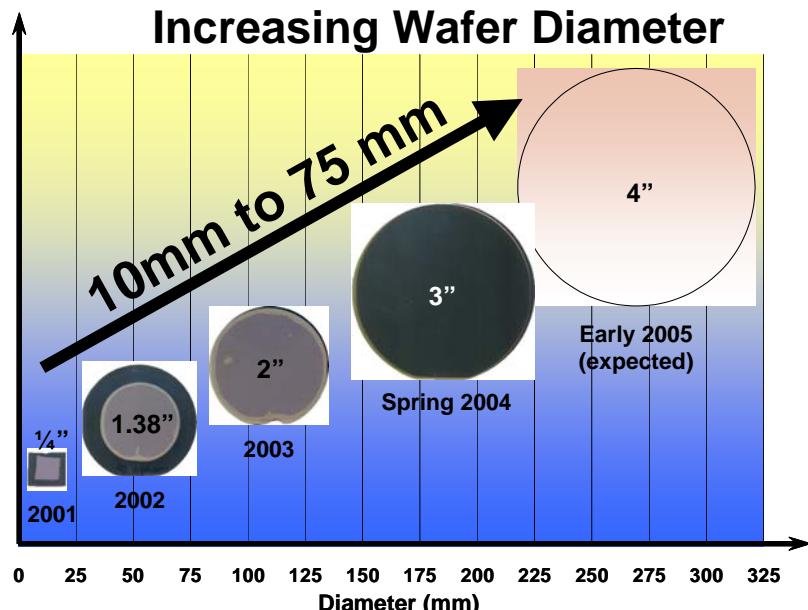
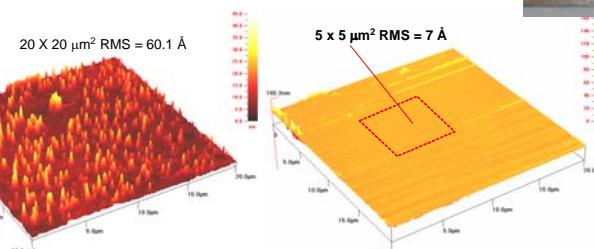
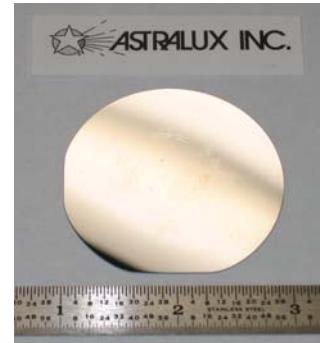


ASTRALUX, INC.

Randolph E. Treece



**High-Quality, Low-Cost
HPSI SiC Hybrid
Substrates**

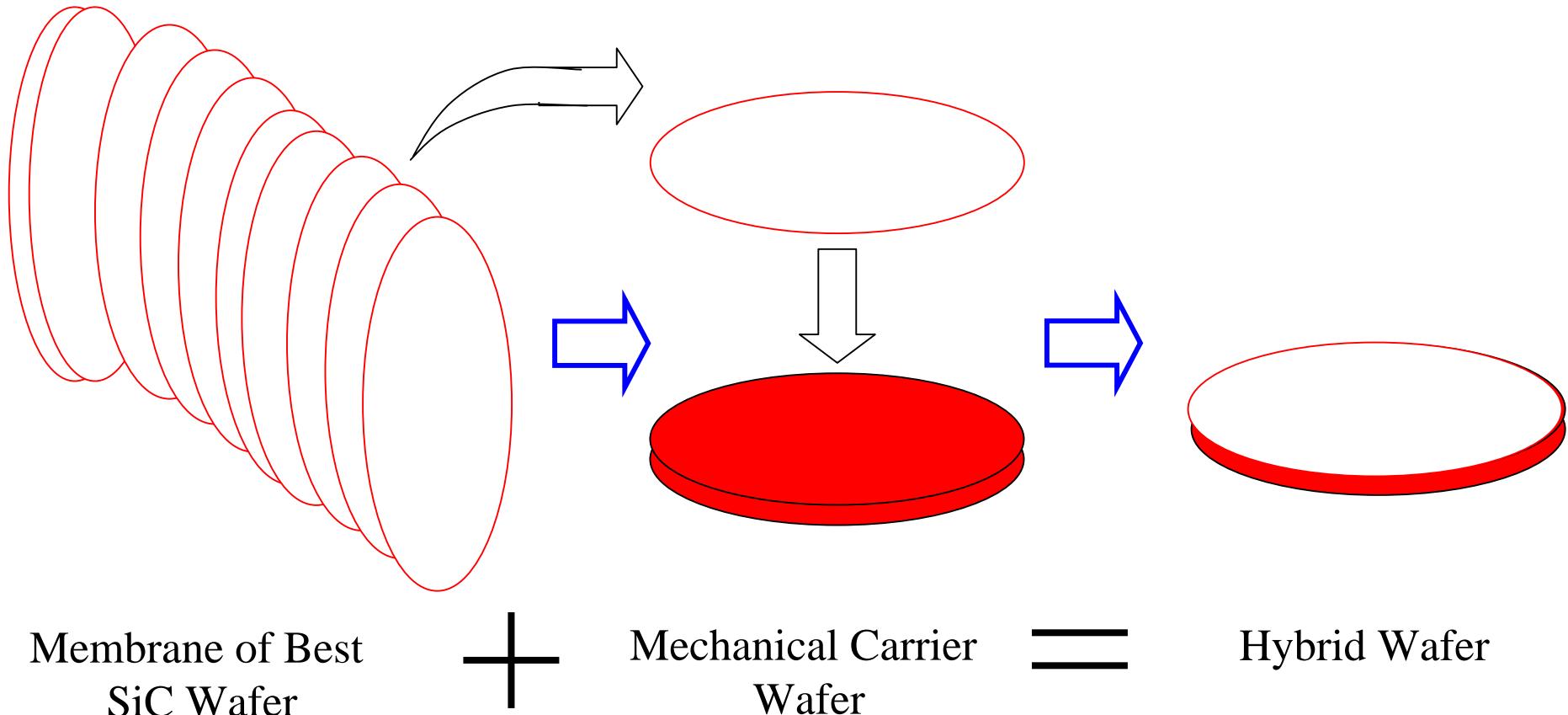


RANDOLPH TREECE
Astralux, Inc.
2500 Central Ave.
Boulder, CO 80301
Ph: 303-413-1440
FX: 303-413-1465

RTREECE@ASTRALUXINC.COM
WWW.ASTRALUXINC.COM

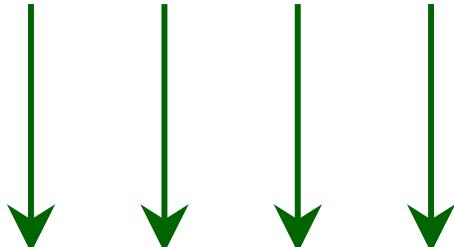
Hybrid Wafer Concept

- Membranes of Low-Defect SiC are attached to inexpensive carrier wafers to form a low cost alternative to bulk SiC.

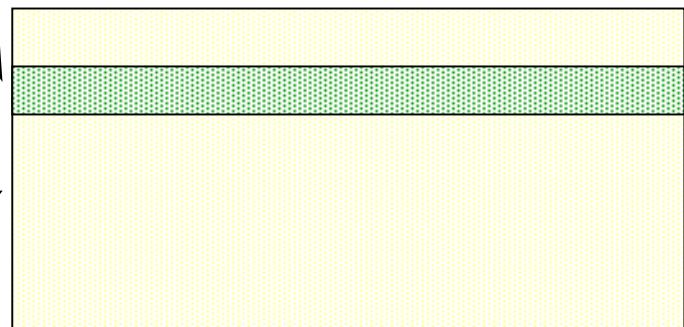


Hybrid Wafer Process (US pat. # 6,699,770)

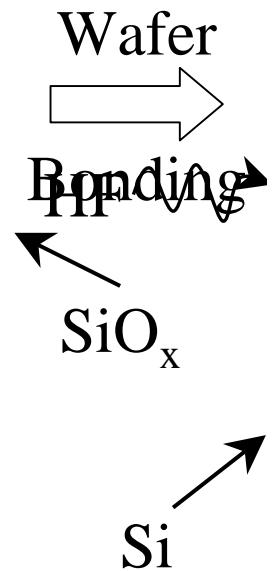
O^+ Implantation



SiC



Hybrid Wafer



High-Quality Hybrid Wafer Surface

- AFM images of a SiC/Si hybrid wafer surface before and after a chemical mechanical polish (CMP). Polishing done in collaboration with Prof. Mark Goorsky at UCLA.
- Final surface is better than 1nm RMS roughness.

