

Cree, Inc. Information

- Cree, Inc. is the world leader in SiC substrates and epitaxy.
- High quality substrates and high voltage epi are available for sale to all contractors
- Cree is the leading manufacturer of SiC power devices in the US.
- Demonstrated voltage and highest power SiC power devices to date

Area of Expertise

- Design and fabrication of high voltage, high power SiC diodes and switches
- SiC device modelling
- Electrical characterization of V_f drift and full reliability testing
- Material growth solutions for decreasing electrically active defects in SiC

Previous Relevant Accomplishments

- Developed low defect SiC epi process for reducing V_f degradation on PiN Diodes
- Demonstrated > 9 kV, 50 A PiN diode
- Demonstrated 67% yield for 10 kV diodes with <100 mV V_f drift
- Demonstrated 10 kV, 123 m Ω -cm² SiC DMOSFET

Contact Information

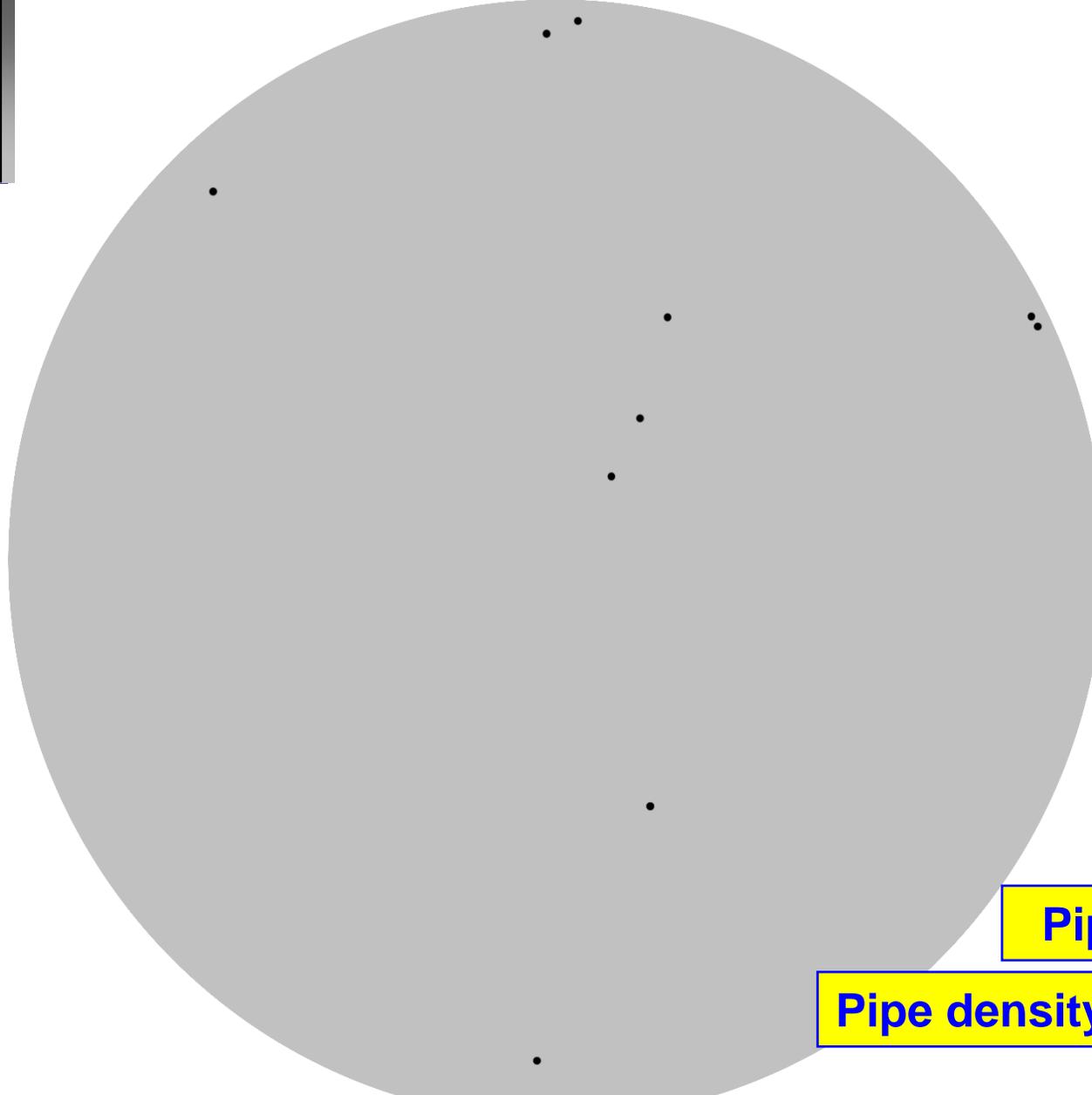
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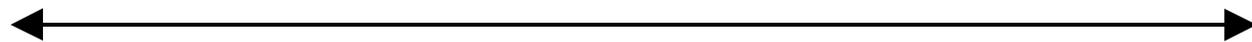
FAX: (919) 313-5787

e-mail: john_palmour@cree.com



Pipes = 10

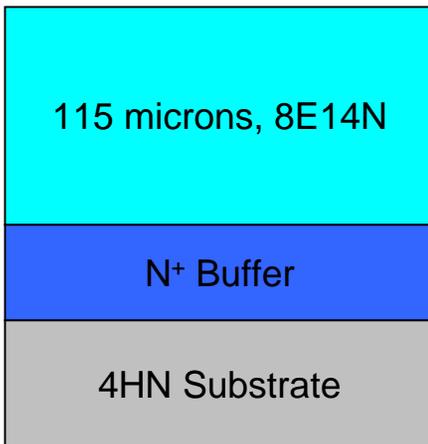
Pipe density = 0.22 cm⁻²



3-inch

Cree's proposed DARPA standard low defect epitaxy offering

Generic 10 kV MOSFET epiwafer



Median critical properties:

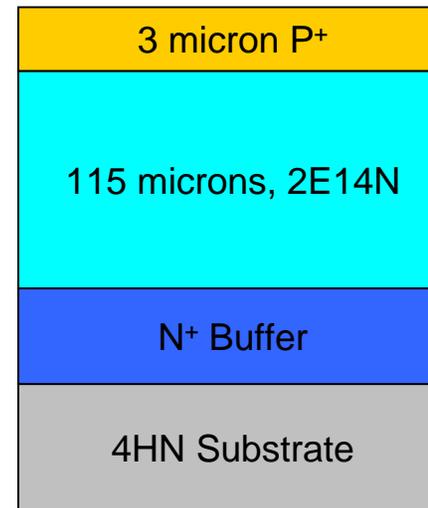
Catastrophic defect density* $< 3 \text{ cm}^{-2}$

Epilayer thickness variation $< 2.5 \%$

Epilayer doping variation $< 10 \%$

**Carrot defect reduction process*

Generic 10 kV PiN diode epiwafer



Median critical properties:

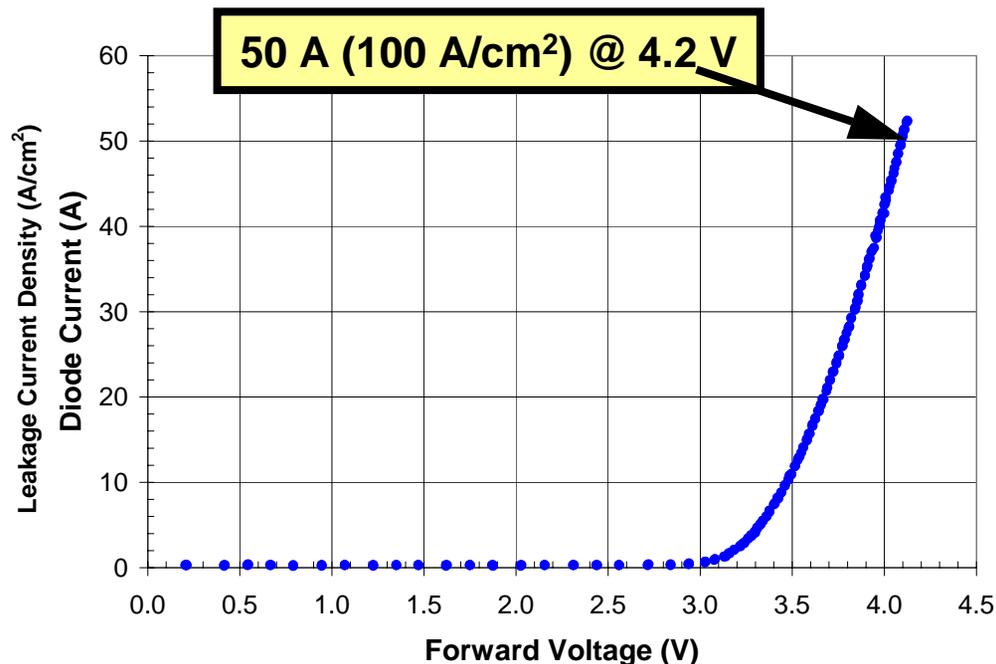
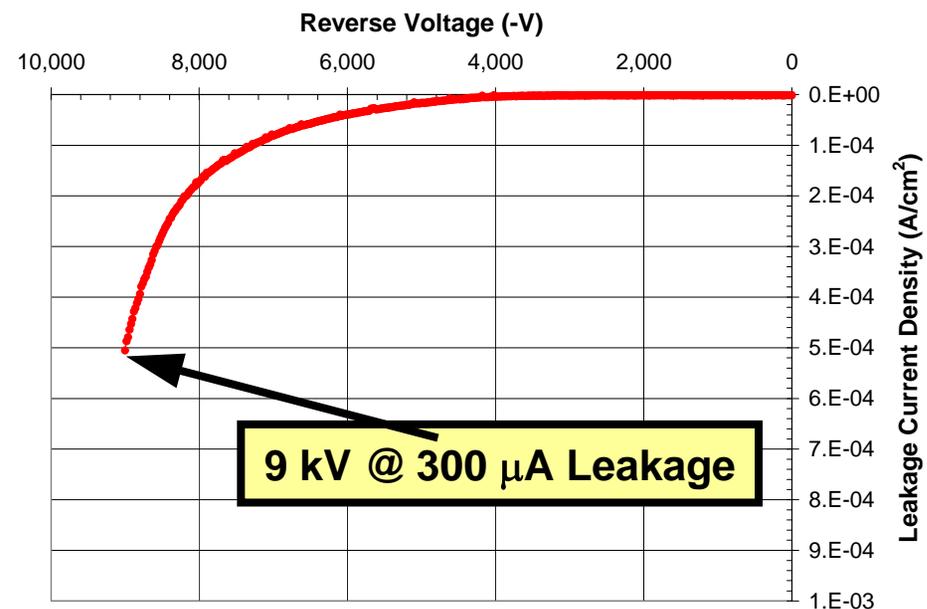
Basal plane dislocation EPD* $< 30 \text{ cm}^{-2}$

Epilayer thickness variation $< 2.5 \%$

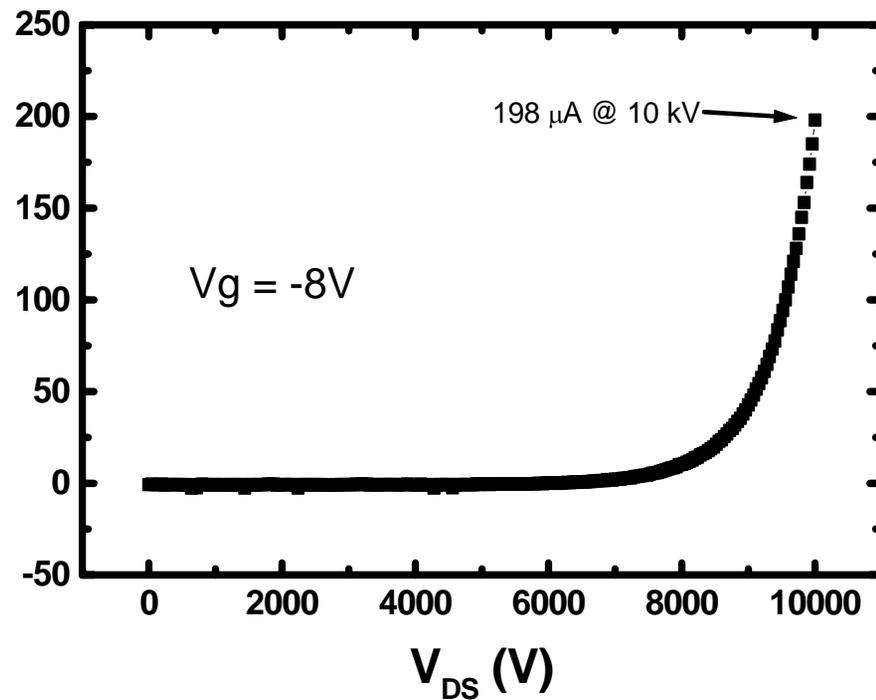
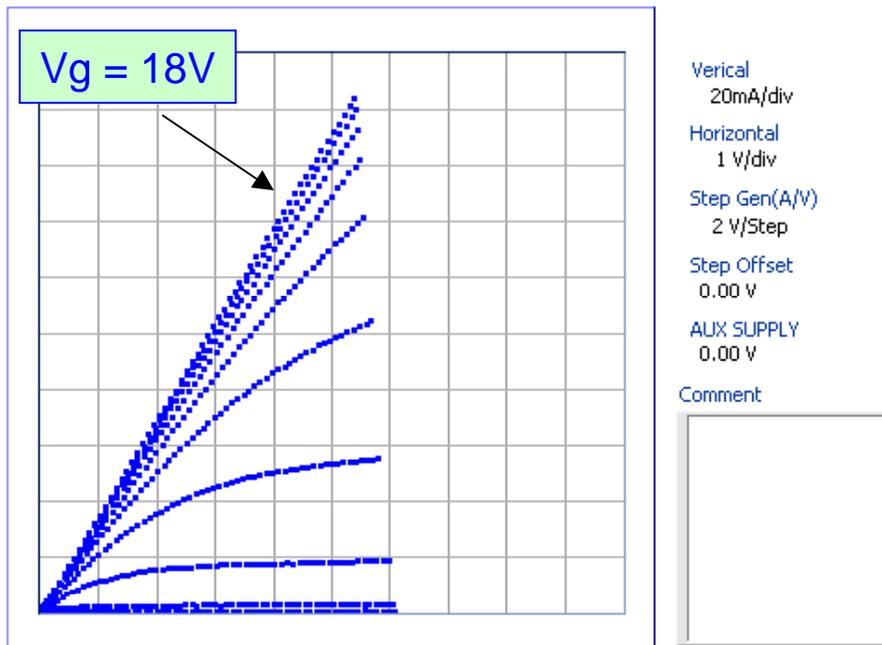
Epilayer doping variation $< 10 \%$

**Carrot defect reduction process &
Basal plane dislocation reduction process*

Forward and Reverse I-V on the Largest SiC Chip Made Yet!



- Reverse blocking is current compliance limited
- 100 μm , Low BPD Epitaxy
- V_f drift < 100 mV after 100 hours
- 8.5 mm x 8.5 mm total chip area



$$R_{ds(on)} = 123 \text{ m}\Omega\text{-cm}^2!!$$

Blocking Voltage = 10 kV
 $J_{leakage} = 6.5 \text{ mA/cm}^2$