

DARPA/MTO IMAGING COHERENT OPTICAL RADAR (ICHOR)

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DARPA/MTO**

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MAYO SPECIAL PURPOSE PROCESSOR DEVELOPMENT GROUP (SPPDG) - 1

- **Research group within the Mayo Foundation (Not-for-profit organization for Health Care/Research/ Education)**
- **Specializes in developing and demonstrating cutting edge, high performance technologies for DoD applications**
- **Transfer technology to Mayo clinical and research environment when applicable**

MAYO SPECIAL PURPOSE PROCESSOR DEVELOPMENT GROUP (SPPDG) - 2

- In existence since 1971, all funding presently from DoD sources
- Resource for government and industry due to long corporate memory
- Unbiased, neutral-party technology developers
- We are non-competitive with corporations

MAYO'S ROLE IN DARPA PROGRAMS

- Mayo collaborative efforts are not costed against contractors in DARPA programs
- Tasks typically performed under DARPA funding
 - Testing in an unbiased, non-competitive environment
 - Identification and exploitation of possible project synergies
 - Identification of potential benefits to the military system user community
 - Risk reduction through test structure/circuit design and simulation

MAYO'S RECENT ROLE IN ACTIVE AND PASSIVE IR PROGRAMS

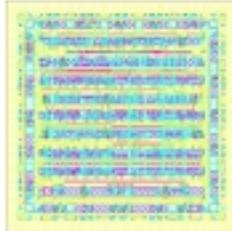
- **3D Imaging program**
 - Characterization of avalanche photo diodes (APDs)
 - InGaAs
 - HgCdTe
 - Signal integrity
 - Design and fabrication of S/H break out macro
 - Analysis of low noise wide bandwidth TIA
- **Vertically Interconnected Sensor Array Program**
 - Electromagnetic simulation
 - Signal integrity
 - Test site design & test

SPPDG TECHNOLOGY AREAS OF EXPERTISE - 1

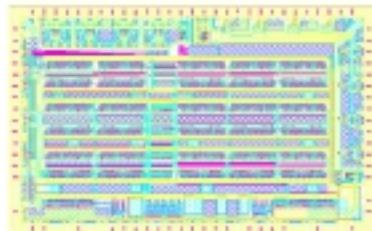
- **Integrated circuit design and test**
 - **Technologies - GaAs, InP, SiGe, SOI, silicon**
 - **Standard devices - HBT, HEMT, BiCMOS, CMOS**
 - **Advanced technologies - Antimonides, GaN, SiGe MODFET**
 - **Analog, digital, and mixed signal circuits**
 - **Over 150 circuits designed since 1983**

MAYO CIRCUITS IMPLEMENTED IN IBM SiGe BiCMOS TECHNOLOGY ON DARPA MULTI USER MASKSET 2

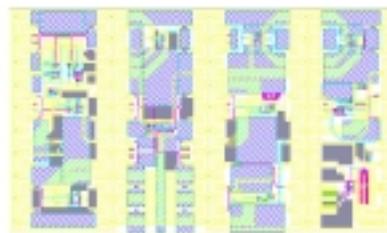
BIPOLAR
4:1 MUX / 1:4 DEMUX



BIPOLAR
CML/ECL TRANSLATORS AND
32-BIT SHIFT REGISTER

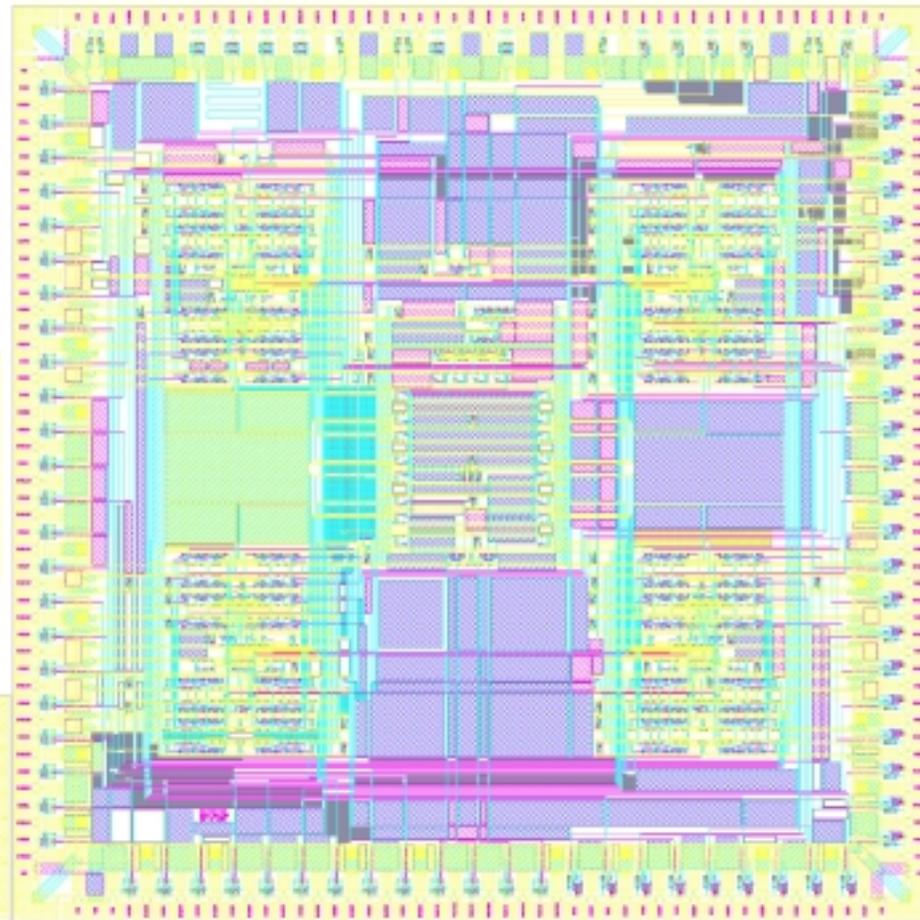


BREAKOUT MACROS



BICMOS BIPOLAR CMOS

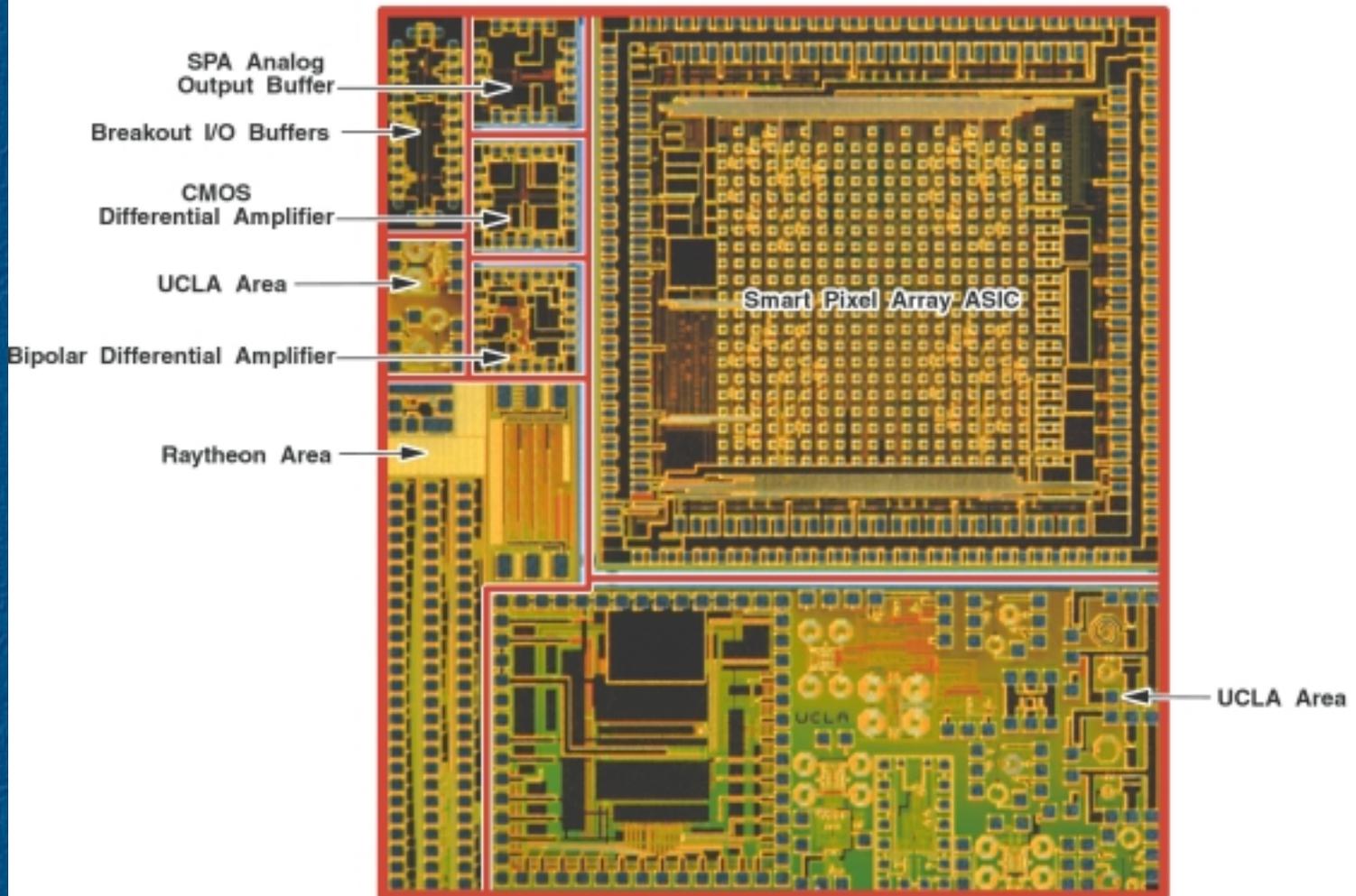
BiCMOS
32:4 MUX / 4:32 DEMUX



04 / 1999 / BAR / 16212



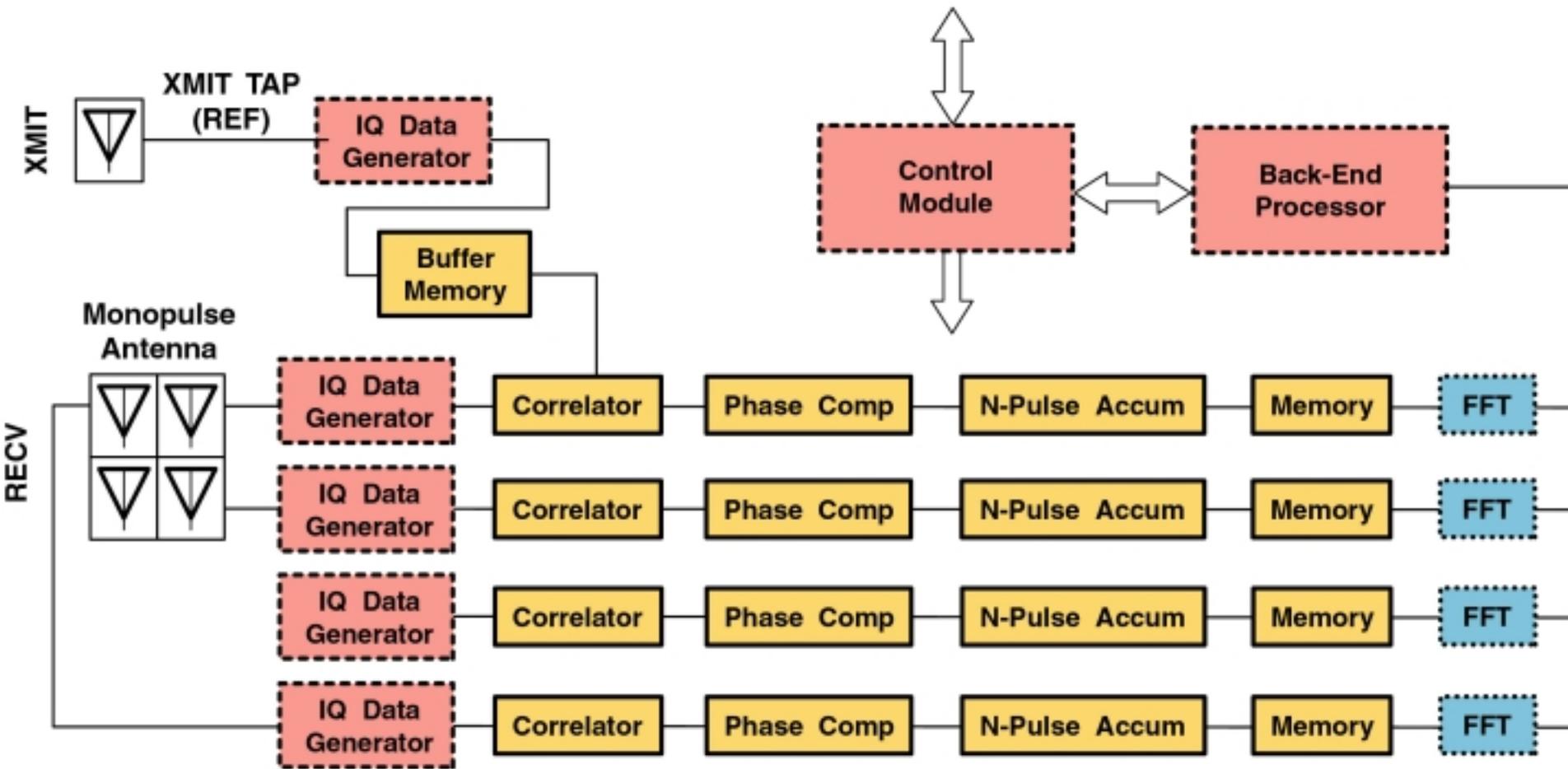
PHOTOGRAPH OF MAYO / SPAWAR MULTI-PROJECT
WAFER RUN #2 (MPW-2) IMPLEMENTED IN
IBM SiGE BiCMOS 7HP PROCESS (0.18 μm CMOS FETS, 120 GHz f_T HBTs)



06 / 2001 / GJF / 17700



NOISE CORRELATION RADAR (NCR) SYSTEM BLOCK DIAGRAM



- China Lake
- MIT Lincoln Labs
- Mayo

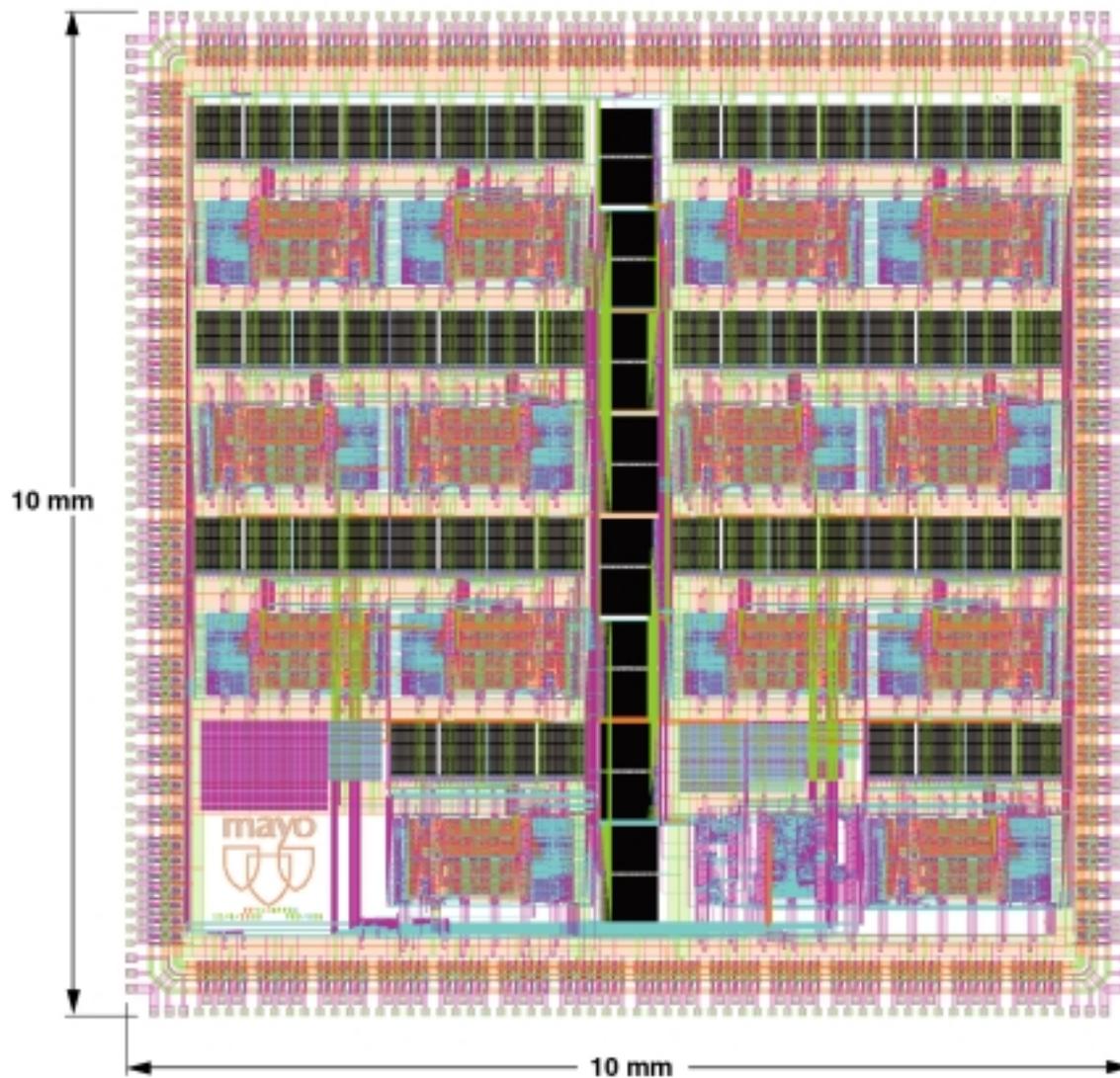
04 / 1999 / PRS / 16181



BLOCK LAYOUT OF PIPELINED FAST FOURIER TRANSFORM (FFT) CHIP TARGETED FOR LSI LOGIC +3.3V/+2.5V 0.25 μm BULK CMOS TECHNOLOGY



FINAL LAYOUT OF MAYO DESIGNED PIPELINED FAST FOURIER TRANSFORM (FFT) CHIP
LSI LOGIC +3.3 V / +2.5 V 0.25 μ m BULK CMOS TECHNOLOGY



02 / 2001 / SMC / 17470



SPPDG TECHNOLOGY AREAS OF EXPERTISE - 2

- **Electronic packaging design and characterization**
 - **Printed circuit boards**
 - **Multi chip modules**
 - **Test fixtures**
 - **Probe cards**
 - **Digital, mixed signal, optoelectric**

SPPDG TECHNOLOGY AREAS OF EXPERTISE - 3

- **Assembly and test laboratories**
 - ~2900 square feet class 1000 test laboratory
 - ~1500 square feet class 100 assembly laboratory
 - Wire and flip chip bonders
 - Digital pattern generation up to 20 GHz
 - Vector network analyzer measurements up to 220 GHz
 - Novel fixturing and probing techniques
 - Cross sectioning, SEM
 - Wafer thinning and dicing
 - Temperature forcer
 - Anechoic chamber

**MAYO FOUNDATION SPPDG's CLASS 100 ASSEMBLY CLEAN ROOM, NORTH BAY
(Lefthand Side: Two Manual Die Bonders, Manual Wire Bonder, Hot Gas Rework Station,
Ball Grid Array Assembly Station, Ball Grid Array Rework Station, Production-Rated
Palomar Model 3500 Fully Automatic Pick-And-Place Machine; Righthand Side: Wafer Dicing Saw,
Wafer Tape Expander, Wafer Scriber, General Inspection Microscope, Wide-Field
Measurement Microscope, High-Magnification Measurement Microscope, Lead Forming Station)**



MAY_22 / 2003 / BKG / 19084

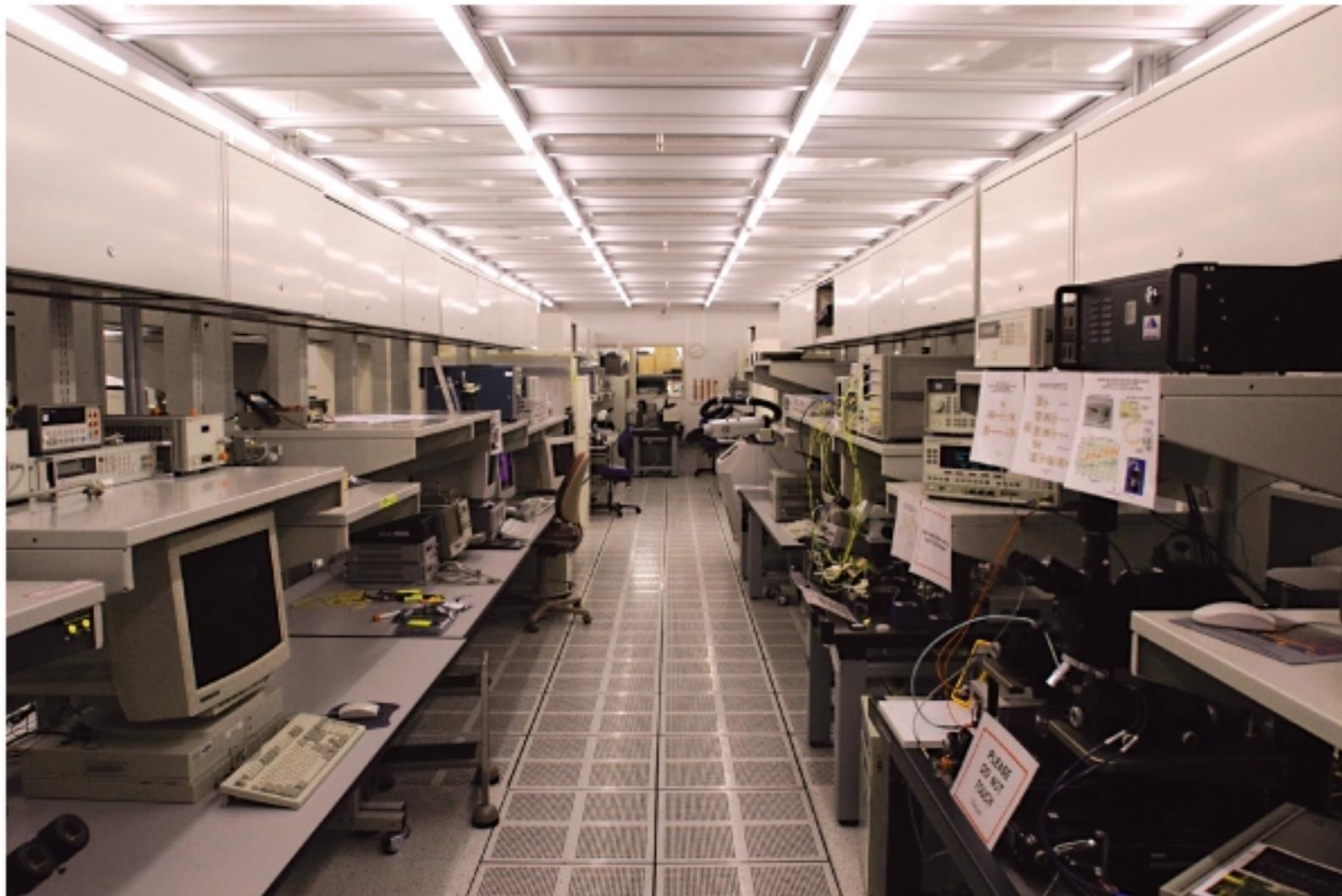


KARL SUSS FC - 150 FLIP CHIP DIE BONDER
(Flip Chip Alignment and Bonding / Precision Die Placement and Bonding,
1 - 3 Micron Overlay Accuracy with Up to 50 kg of Force;
Operating Temperatures 25° - 450° C)



MAYO FOUNDATION SPPDG's CLASS 1000 TEST CLEAN ROOM

(Middle South Bay of Four-Bay Facility, Currently Assigned to: TFAST Indium Phosphide Divider Test Suite, LADAR Infrared Staring Array Test Suite, Temperature Forcing Unit, 45 MHz-110 GHz Vector Network Analyzer, High Speed Serial Link Test Station, and Several Laboratory Computers)



MAY_22 / 2003 / BKG / 19083



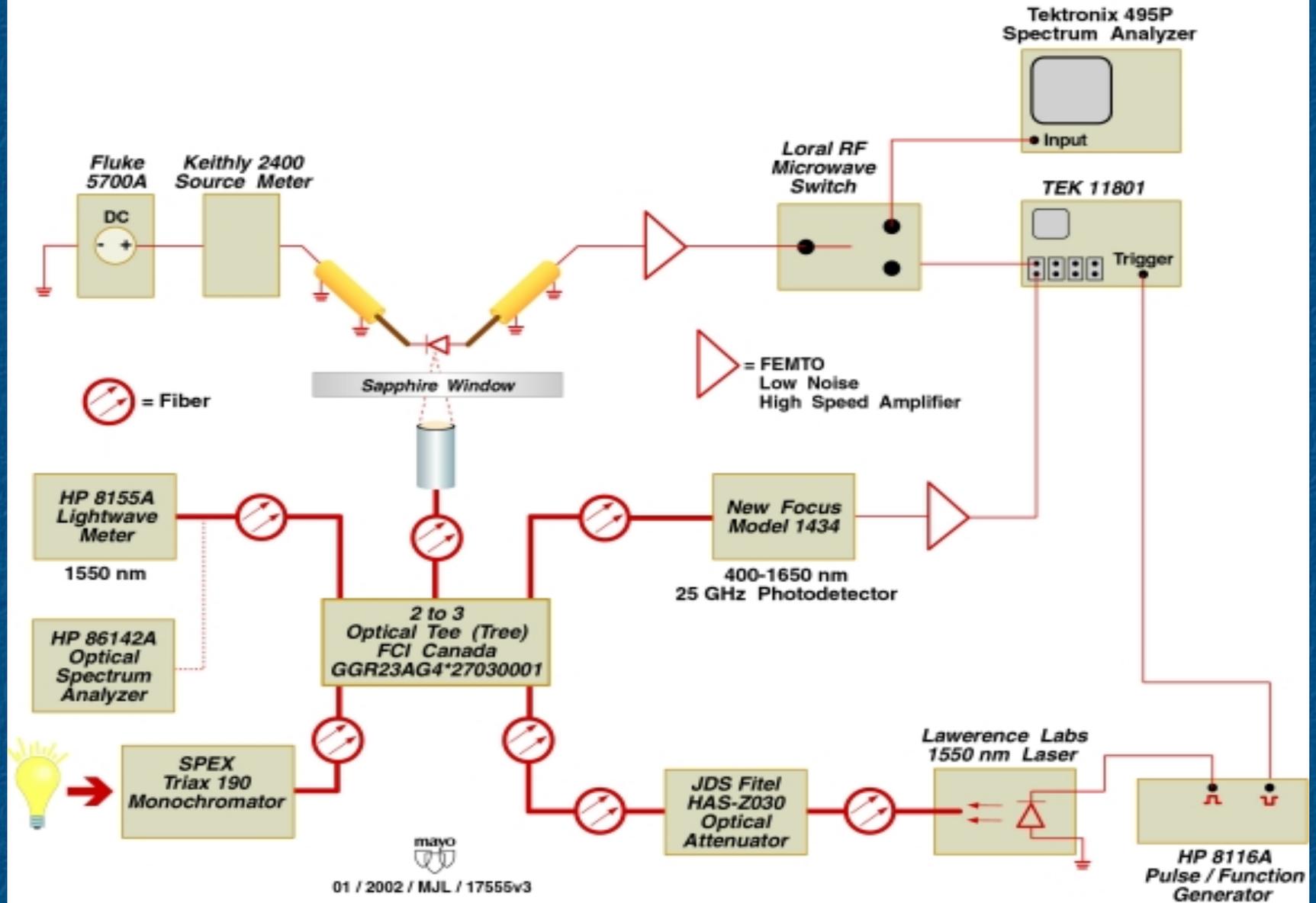
**PHOTOGRAPH OF LABORATORY HARDWARE
FOR TESTING OF OPTICAL TO ELECTRICAL TRANSDUCER ARRAYS
(Work Performed for DARPA / MTO 3D Imaging Program)**



05 / 2001 / MJL / 17664



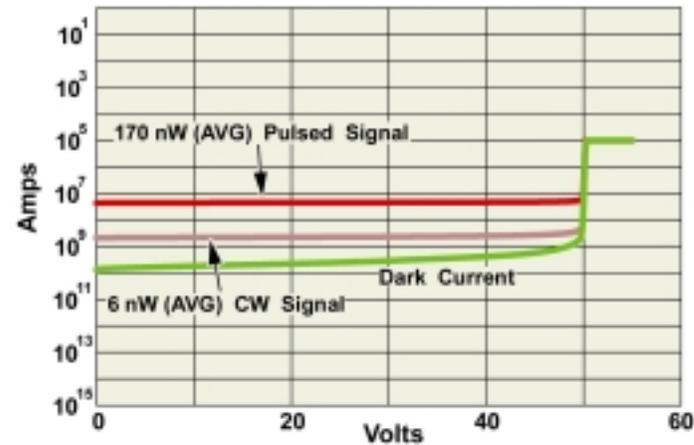
TEST SUITE USED FOR PHOTODETECTOR CHARACTERIZATION (APD Array Used As Example)



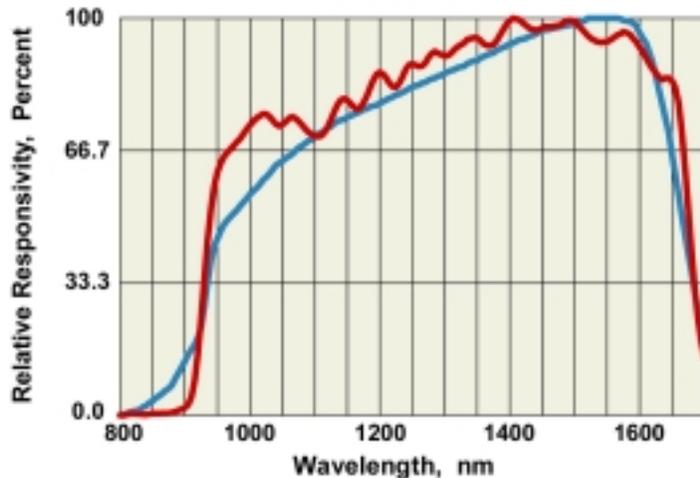
OPTICAL TO ELECTRICAL TRANSDUCERS FOR 3-D IMAGING PROGRAM
 (Commercial EG&G InGaAs C30644ECER Avalanche Photo Diode
 [Rated for Operation Between 1100 nm to 1700 nm])



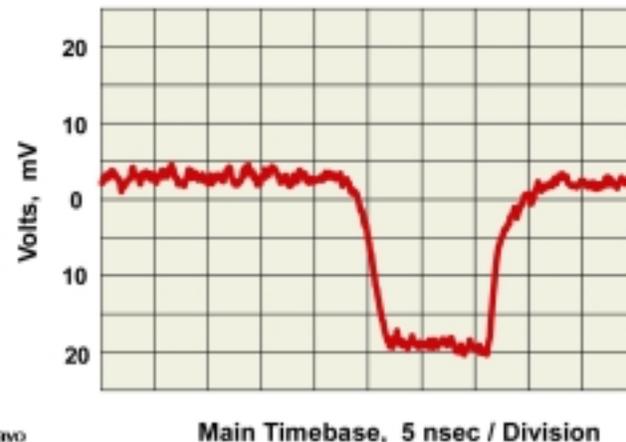
IV RESPONSE CURVES
 (Light Source 1550 nm Laser)



DC RESPONSIVITY



AC RESPONSE

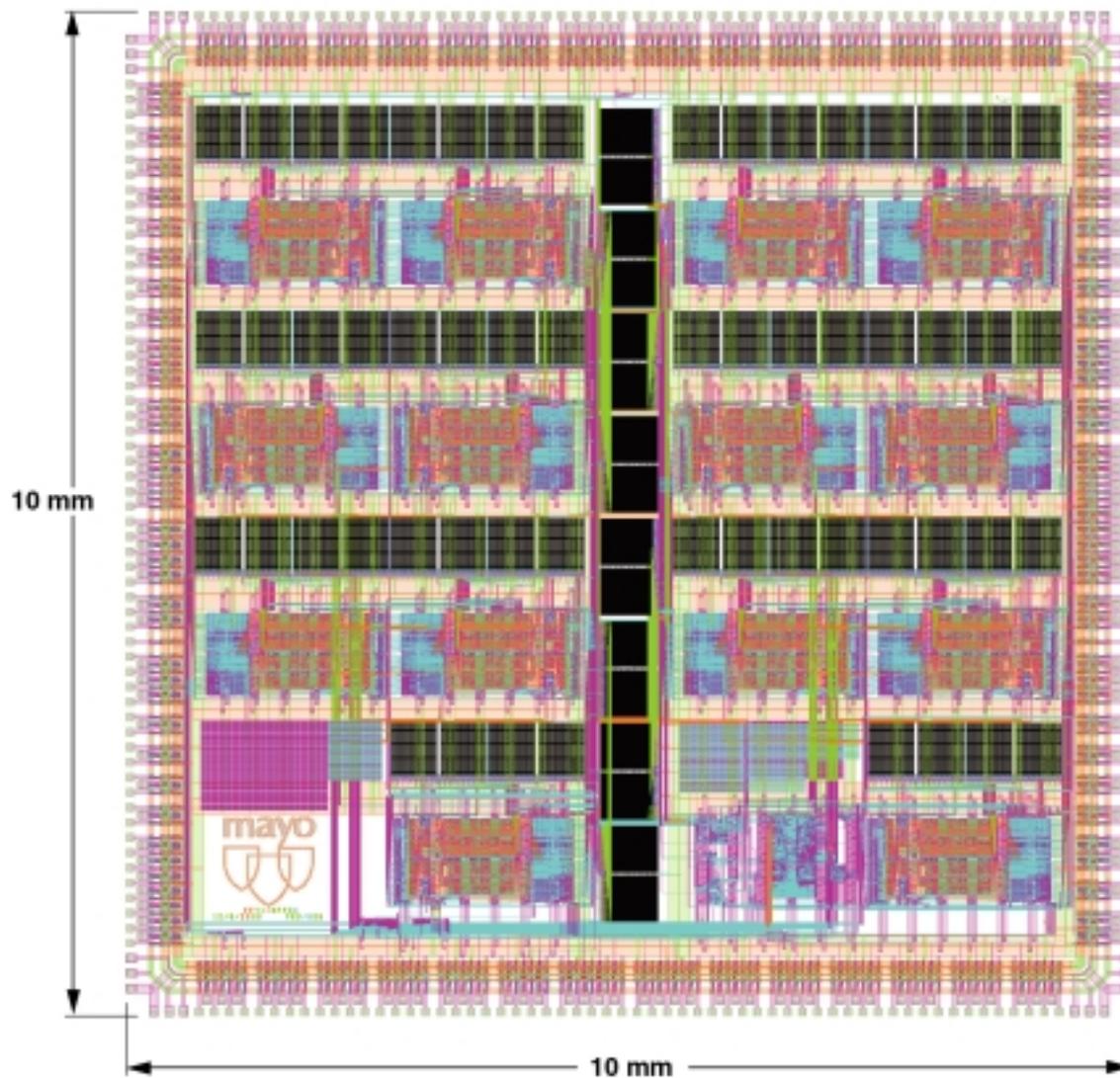


03 / 2002 / MJL / 18246

SPPDG TECHNOLOGY AREAS OF EXPERTISE - 4

- **Simulation and modeling of ICs, MCMs, PCBs, and packages**
 - **Circuit level (HSpice, ADS, Spectre)**
 - **Digital logic level (Verilog, VHDL)**
 - **Timing verification (Verilog, VHDL)**
 - **Electromagnetic modeling (In house, HFSS, Momentum, FEMLAB)**
 - **Device model generation (IC-CAP)**

FINAL LAYOUT OF MAYO DESIGNED PIPELINED FAST FOURIER TRANSFORM (FFT) CHIP
LSI LOGIC +3.3 V / +2.5 V 0.25 μ m BULK CMOS TECHNOLOGY

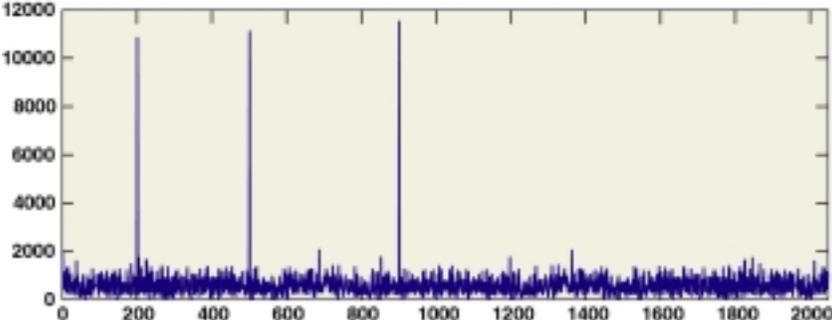


02 / 2001 / SMC / 17470

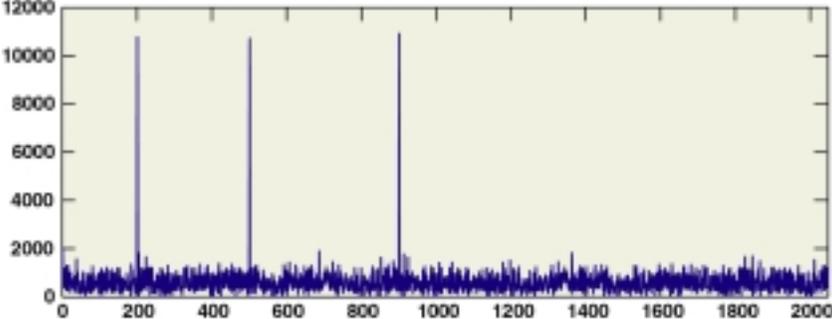


**COMPARISON OF SIMULATED RESULTS TO MAYO DESIGNED
PIPELINED FFT CHIP MEASURED RESULTS
(1 x 2048 Point Fast Fourier Transform)**

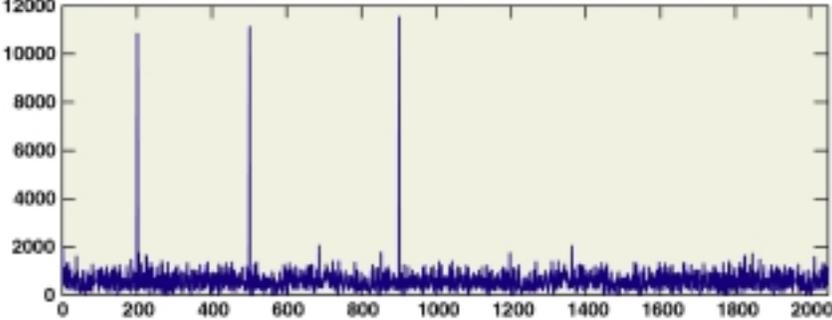
Matlab Double Precision Floating Point FFT Results Magnitude



FFT Chip IC (Simulated) Fixed Point Output Magnitude

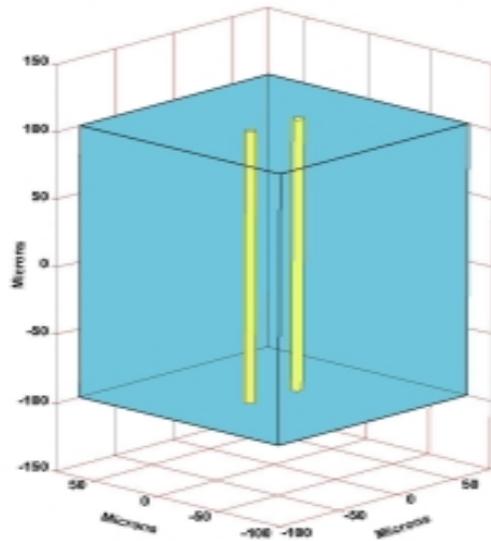


FFT Chip IC (Measured) Fixed Point Output Magnitude

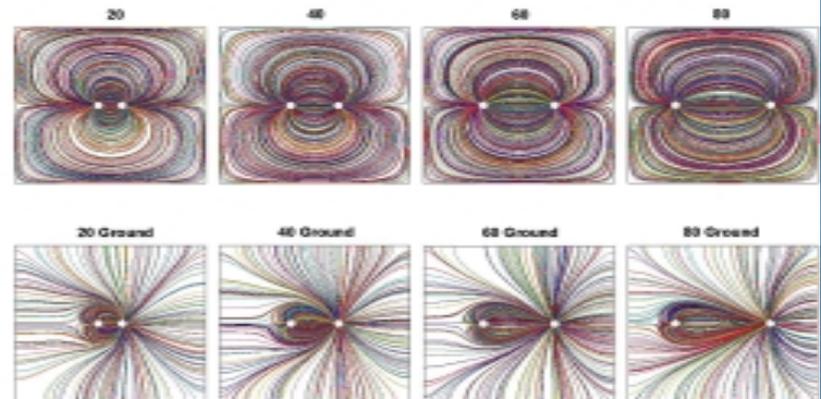


COMPARISON OF ELECTROMAGNETIC SIMULATIONS OF VIA TO VIA COUPLING (Vertically Integrated Sensor Array (VISA) Program)

RENDERED VIEW OF SIDE BY SIDE VIAS
(200 Microns In Length, 8 Microns In Diameter)



ELECTRIC FIELD OF VARIOUS VIA SPACING



CALCULATION OF CAPACITANCE FROM ELECTRIC FIELD ENERGY

$$C = \frac{1}{2} \frac{W_e}{V^2}$$

$$W_e = \text{Electric Field Energy} = \int_{\text{Volume}} \left(\int_0^D \vec{E} \cdot d\vec{D} \right) dv$$

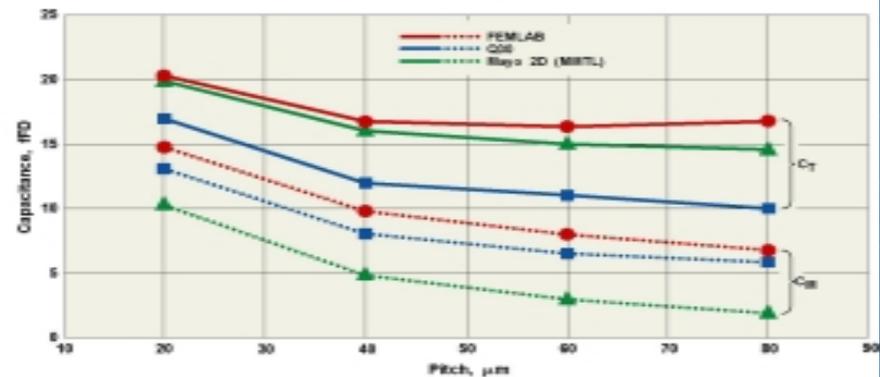
V = Voltage Potential Between Plates

C = Capacitance



SEP_16 / 2003 / MJL / 19363

PLOT OF TOTAL AND MUTUAL CAPACITANCE FOR
2-8 μm DIAMETER, 200 μm LONG VIAS AS A FUNCTION OF PITCH





Mayo Clinic SPPDG