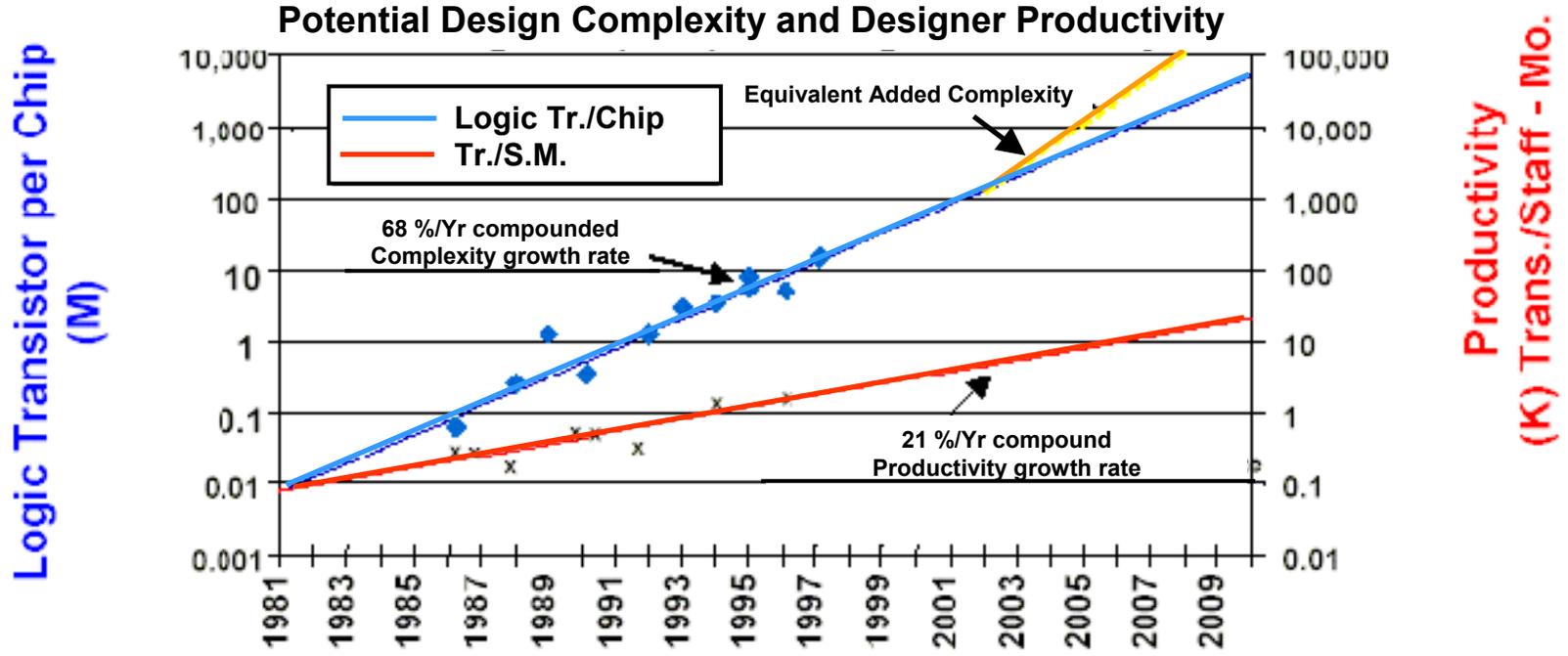




***The MARCO/DARPA
Gigascale Silicon Research Center
Introduction and Overview***



The Productivity Gap



<u>Year</u>	<u>Technology</u>	<u>Chip Complexity</u>	<u>Frequency</u>	<u>3 Yr. Design Staff</u>	<u>Staff Cost*</u>
1997	250 nm	13 M Tr.	400 MHz	210	90 M
1998	250 nm	20 M Tr.	500	270	120 M
1999	180 nm	32 M Tr.	600	360	160 M
2002	130 nm	130 M Tr.	800	800	360 M

* @ \$ 150 k / Staff Yr. (In 1997 Dollars)

Source: SEMATECH

“It’s a Moonshot, Not Rocket Science”

Overall Program Goals

- > 1 Billion transistor chip
- In a technology ~~< 0.1 micron~~ **50nm**
- Using IP from several sources (mixed-signal)
- Running at ~~> 2 GHz~~ on-chip **10GHz**
- With a team of < 30 designers
- In < 6 months
- With competitive cost and power-delay-area product

Proposed GSRC 10-Year Goal, November 1997

GSRC Quarterly Workshops, 2001



- ✓ **March Workshops: an experiment in regional Theme meetings**
 - 3/5: Cadence Labs, Berkeley: Communication-/Component-based Design
 - 3/9: Berkeley Radisson Hotel: Fully-programmable Systems & Self-test of Mixed-signal Systems
 - 3/19-20: CMU, Pittsburgh: Constructive Fabrics and Verification of Concurrent, Component-Based Design
 - 3/31: Stanford Univ.: Power and Energy in Design
- ✓ **June 17th-18th Workshop, Las Vegas Convention Center (at the DAC)**

Theme: “From Ad Hoc System-on-a-Chip to Disciplined Platform-based Design”

Dinner speaker: Dr. Christopher Rowen, CEO Tensilica

“Rethinking the Microprocessor for System-on-a-Chip”
- ✓ **September 6th Annual Review, Intel Site, Santa Clara, CA**

Dinner speaker: Dr. Christopher Hamlin, CTO LSI Logic
- September 7th Workshops, Marriott Hotel, Santa Clara, CA**

Theme: working meetings
- December 2001 Workshop, possibly Washington, D.C.**

Theme: Applications of Principles of Platform-base Design: Three Design Threads

Ongoing Development of Effective Working Relationship With Industry & Government



- ◆ Implemented ***GSRC Industrial Liaison*** program, where GSRC faculty are assigned to work with specific MARCO sponsors

- ◆ **GSRC Visits to Many MARCO Sponsors Over Past Nine Months:**
 - ◆ 10/16 ('00) Motorola SPS, Austin, TX
 - ◆ 3/13 SIA Board Meeting and Press Conference, Washington, D.C.
 - ◆ 4/11 Mentor Graphics, San Jose, CA
 - ◆ 4/26 Cypress Semiconductor, Sunnyvale, CA
 - ◆ 5/9 LSI Logic, Milpitas, CA
 - ◆ 5/17 Advanced Micro Devices, San Jose, CA
 - ◆ 7/9 LSI Logic, at Berkeley, CA
 - ◆ 7/19 FCRP Workshop, SIA Headquarters, San Jose, CA
 - ◆ 7/30 Lucent Technologies, Murray Hill, NJ

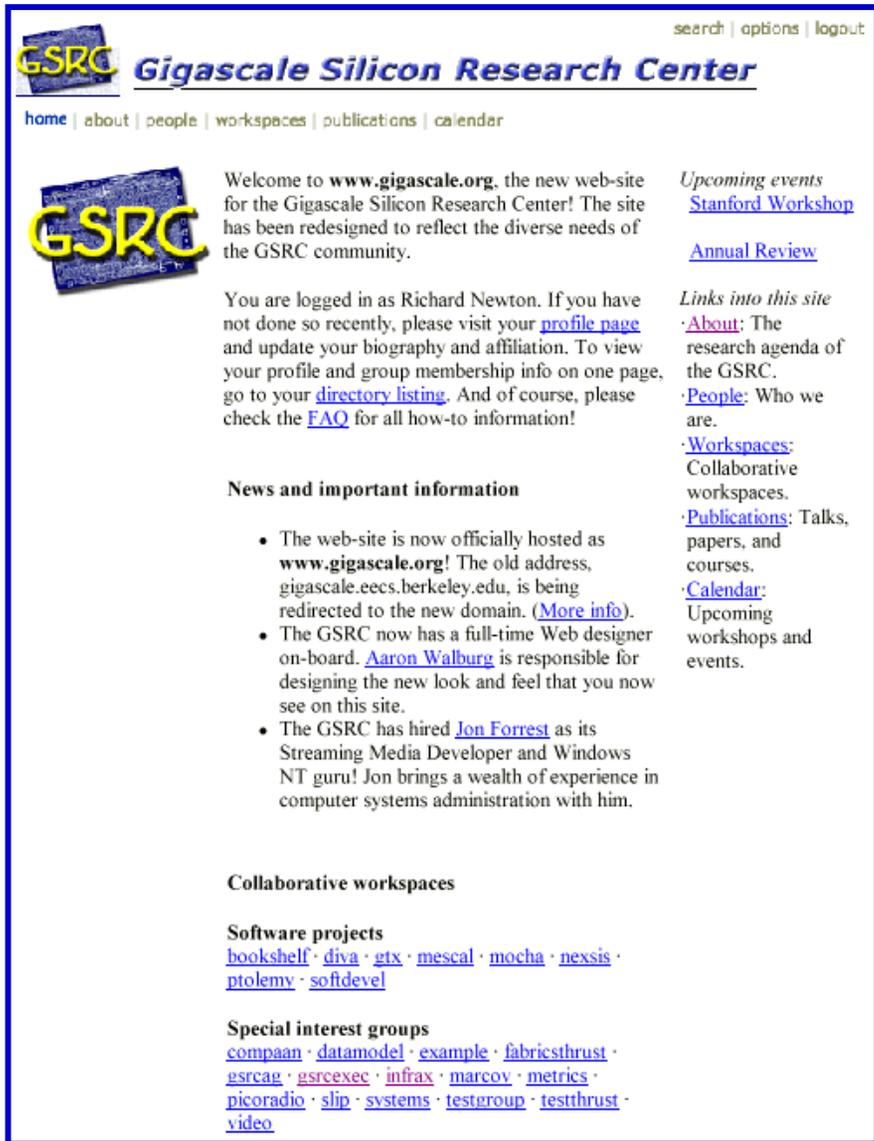
- ◆ Discussion with DARPA management regarding the future role of the FCRP program and leverage for Government programs

Publications and Conference Talks by GSRC Faculty and Students, 2001



- ◆ 5 new Book Titles
- ◆ 19 Refereed Papers in Archival Journals
- ◆ 58 Conference Talks and Proceedings publications
- ◆ 62 papers and talks in the period prior to 1/1/01, bringing the total to 139 since the inception of the Center
- ◆ 6 Major Commercial (Trade) Press Articles on the Work of the GSRC





The screenshot shows the homepage of the Gigascale Silicon Research Center. At the top, there is a navigation bar with links for 'home', 'about', 'people', 'workspaces', 'publications', and 'calendar'. The main content area is divided into several sections: a welcome message, a login status notification, news and important information, collaborative workspaces, software projects, and special interest groups. A sidebar on the right contains links for 'Upcoming events', 'Annual Review', and 'Links into this site'.

GSRC Gigascale Silicon Research Center

search | options | logout

home | about | people | workspaces | publications | calendar

Welcome to www.gigascale.org, the new web-site for the Gigascale Silicon Research Center! The site has been redesigned to reflect the diverse needs of the GSRC community.

You are logged in as Richard Newton. If you have not done so recently, please visit your [profile page](#) and update your biography and affiliation. To view your profile and group membership info on one page, go to your [directory listing](#). And of course, please check the [FAQ](#) for all how-to information!

News and important information

- The web-site is now officially hosted as www.gigascale.org! The old address, gigascale.eecs.berkeley.edu, is being redirected to the new domain. ([More info](#)).
- The GSRC now has a full-time Web designer on-board. [Aaron Walburg](#) is responsible for designing the new look and feel that you now see on this site.
- The GSRC has hired [Jon Forrest](#) as its Streaming Media Developer and Windows NT guru! Jon brings a wealth of experience in computer systems administration with him.

Collaborative workspaces

Software projects
[bookshelf](#) · [diva](#) · [gtx](#) · [mescal](#) · [mocha](#) · [nexsis](#) · [ptolemy](#) · [softdevel](#)

Special interest groups
[compaan](#) · [datamodel](#) · [example](#) · [fabricsthurst](#) · [gsrcaag](#) · [gsrcexec](#) · [infrax](#) · [marcov](#) · [metrics](#) · [picoradio](#) · [slip](#) · [systems](#) · [testgroup](#) · [testthrust](#) · [video](#)

Upcoming events
[Stanford Workshop](#)

Annual Review

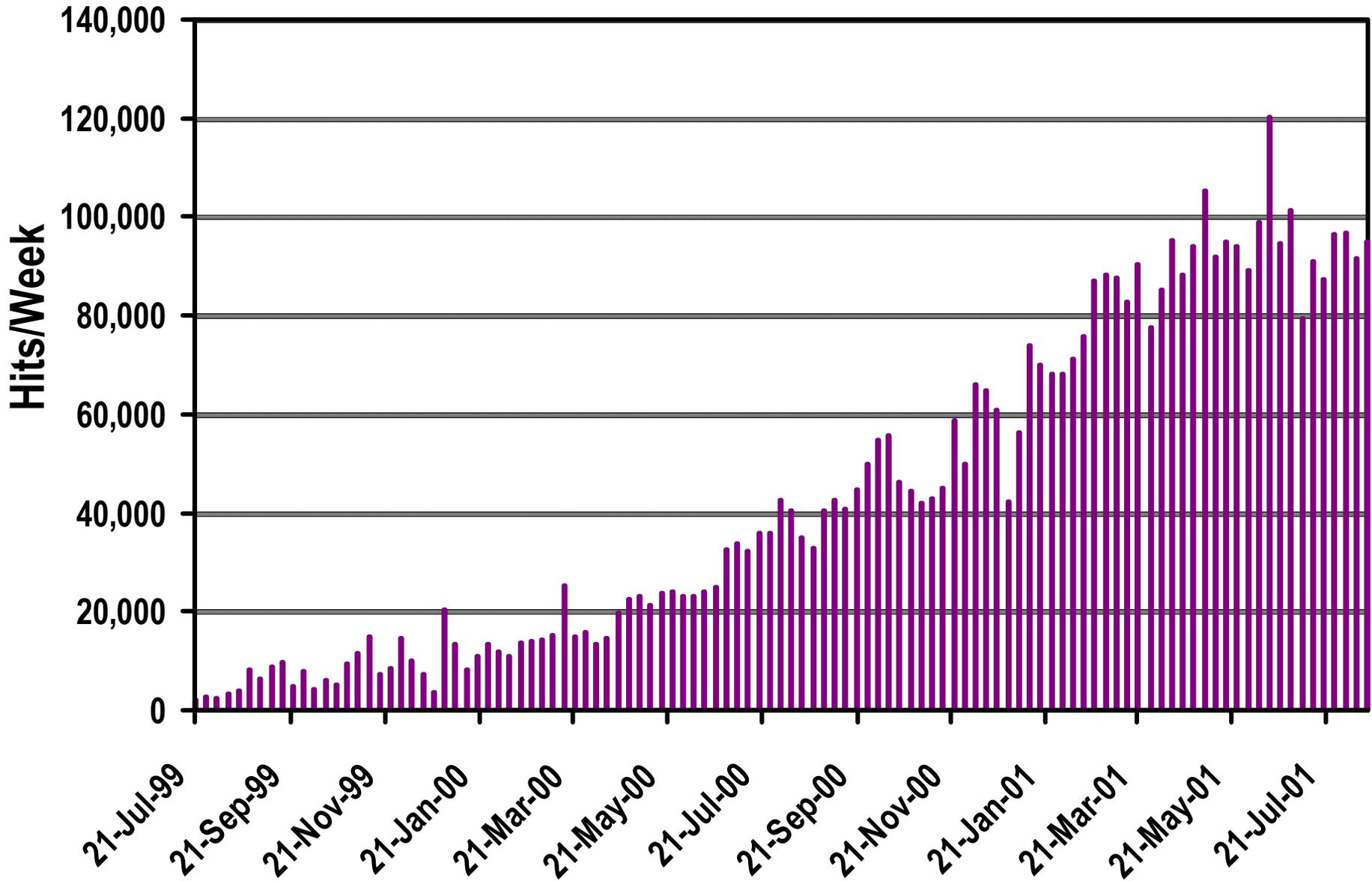
Links into this site
· [About](#): The research agenda of the GSRC.
· [People](#): Who we are.
· [Workspaces](#): Collaborative workspaces.
· [Publications](#): Talks, papers, and courses.
· [Calendar](#): Upcoming workshops and events.

◆ Example: August 2001

56,541 accesses

- ◆ 400841 hits
- ◆ Average visit 3 pages
- ◆ Served 755 Mbytes
- ◆ Broad range of users:
 - ◆ 29% from *com*
 - ◆ 9.2% from *edu*
 - ◆ 1% from *mil, gov*
 - ◆ 21% overseas: 63 countries
 - ◆ France, Canada, Finland, Netherlands, Germany, Hong Kong, Japan heaviest visitors

GSRC Website Statistics: July 1999 – August 2001



GSRC Themes for 2001



Communication/Component-Based Design

A. Sangiovanni
T. Henzinger
E. Lee
R. Newton
J. Rabaey

Fully-Programmable
Systems

K. Keutzer
S. Malik
R. Newton
+ D. August

R. Bryant
E. Clarke
D. Dill
T. Henzinger
K. Sakallah
+ T. Austin
+ T. Reps
+ D. Engler

Self-Test of Mixed-Signal Systems

Validation of Highly Concurrent
Component-Based Designs

Architecture

Microarchitecture

Power and Energy in Design

Constructive
Fabrics

L. Pileggi
A. Kahng
R. Brayton
J. Cong
W. Maly
M. Sadowska
A. Sangiovanni
A. Strojwas
+ H. Schmit

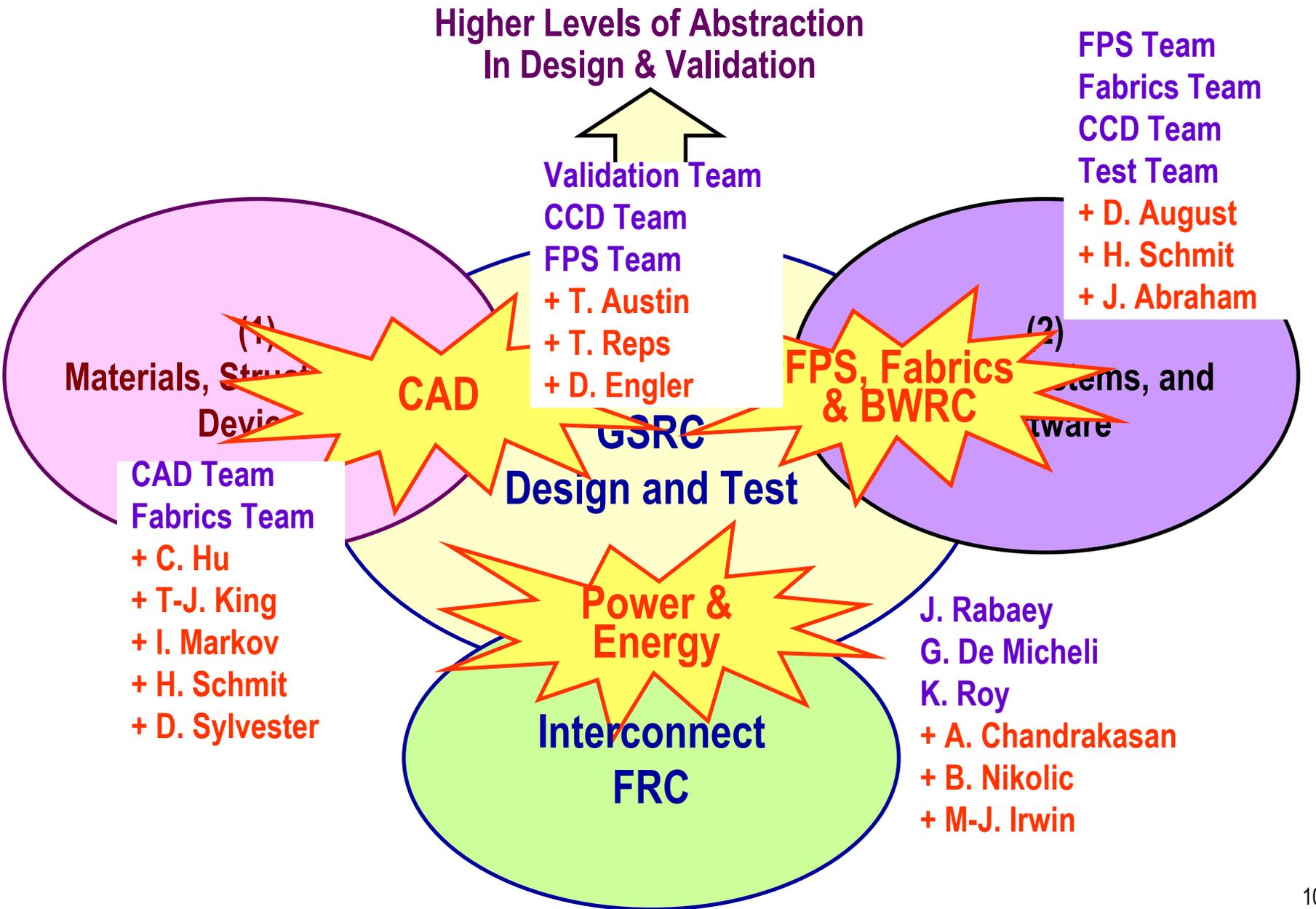
T. Cheng
S. Dey
W. Maly
K. Roy
+ J. Abraham

A. Kahng
W. Dai
W. Maly
L. Pileggi
A. Strojwas
+ C. Hu
+ T-J. King
+ I. Markov
+ H. Schmit
+ D. Sylvester

J. Rabaey
G. De Micheli
K. Roy
+ A. Chandrakasan
+ B. Nikolic
+ M-J. Irwin

Calibrating Achievable Design

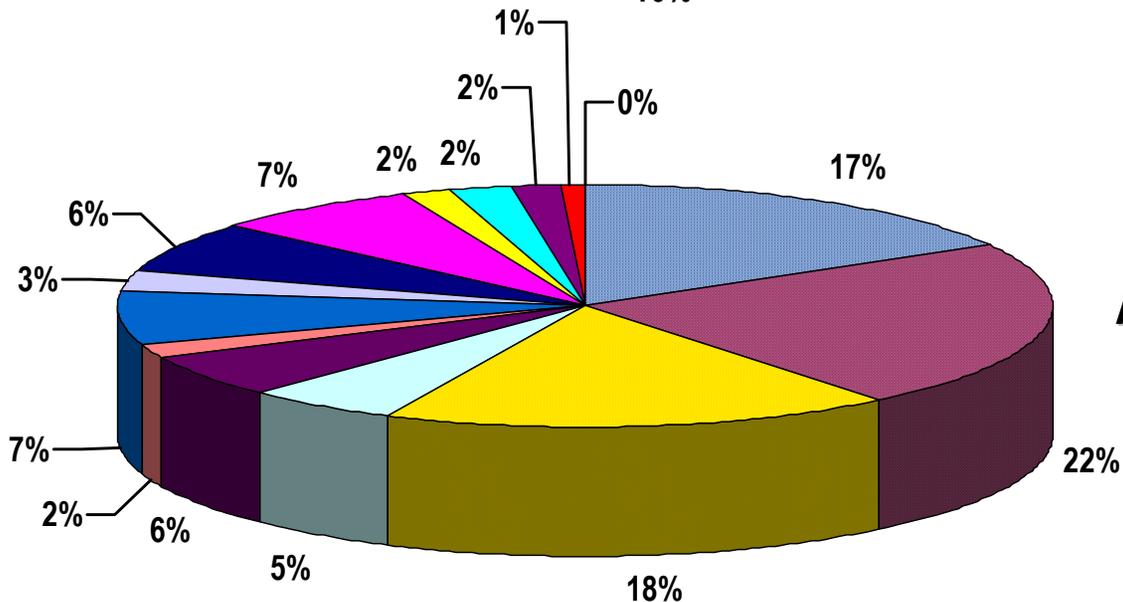
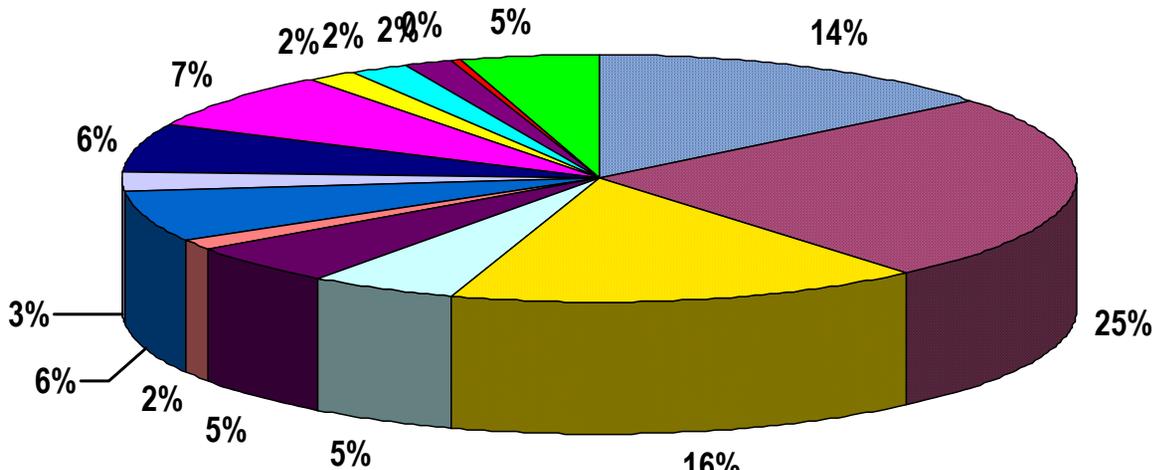
Relationship to Other FRCs and Future Plans



Budget and Projections 2001



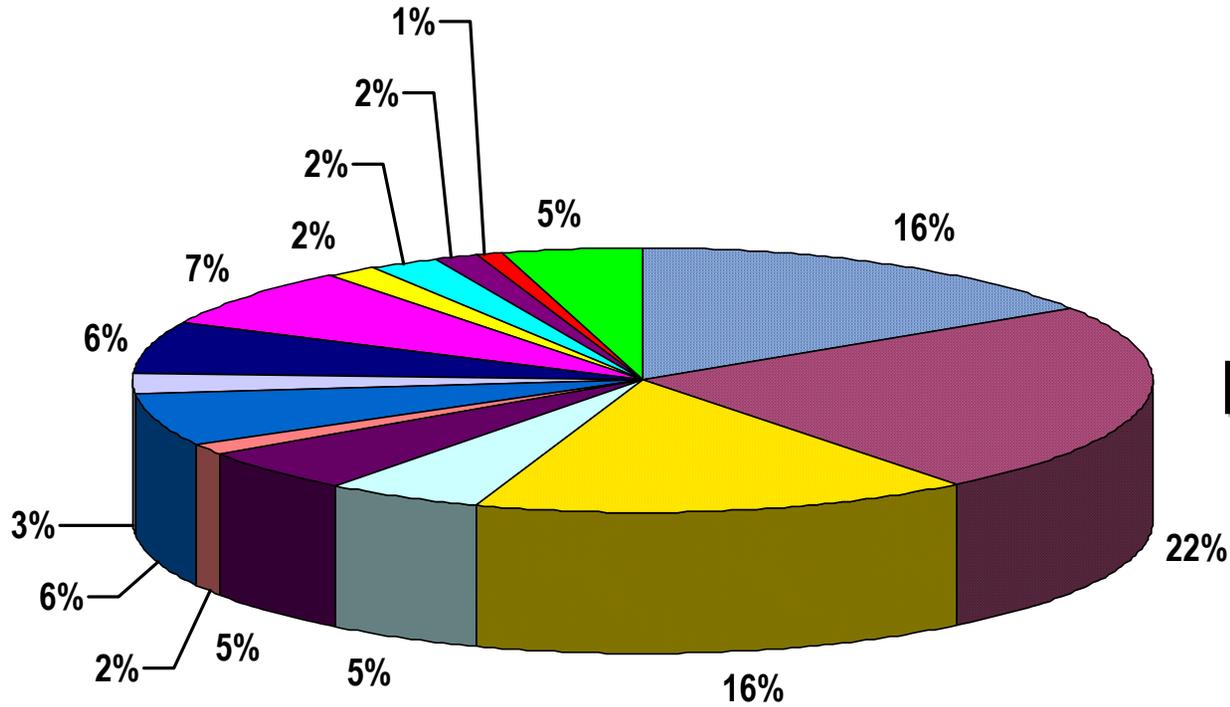
- GSRC
- Berkeley
- CMU
- Michigan
- Princeton
- Purdue
- Stanford
- UCLA
- UCSB
- UCSD
- UCSC
- UT Austin
- Penn State
- Wisconsin
- New Projects



GSRC Budget 2002

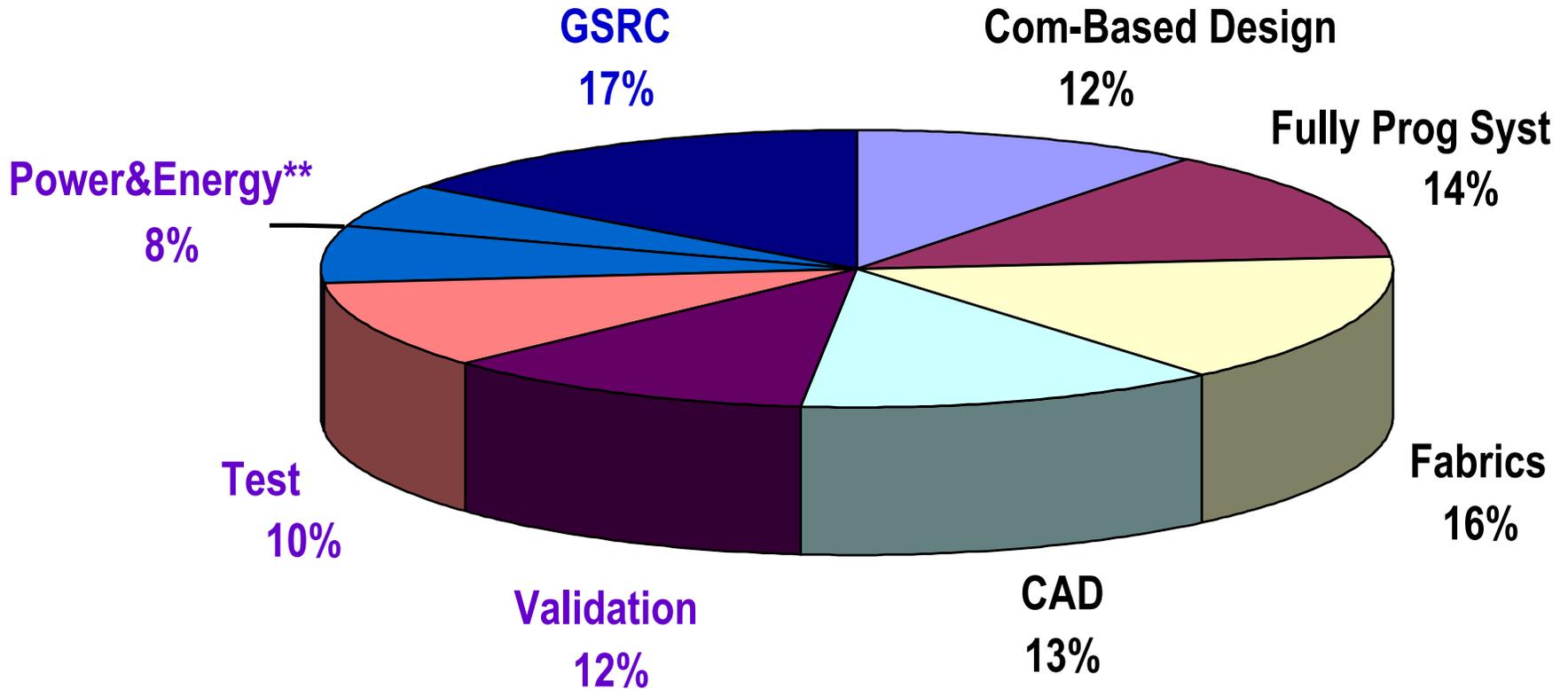


- GSRC
- Berkeley
- CMU
- Michigan
- Princeton
- Purdue
- Stanford
- UCLA
- UCSB
- UCSD
- UCSC
- UT Austin
- Penn State
- Wisconsin
- New Projects



Budget 2002
\$9.9M

Projected Breakdown By Theme: 2001



**Joint with Interconnect FRC

GSRC Research Staff: Current-Proposed



	2001 Actual			2001 Proposed			2002		
	faculty	students	researcher	faculty	students	researcher	faculty	students	researcher
CMU	6	13	1	6	16	1	6	16	2
Michigan	4	4	0	4	5	0	4	5	0
MIT	1	0	0	1	0	0	1	0	0
Penn State	1	3	0	1	3	0	1	3	0
Princeton	2	6	0	3	6	0	3	7	0
Purdue	1	3	1	1	2	1	1	2	1
Stanford	4	5	0	4	5	0	4	6	0
UCB	9	29	5	10	31	7	10	31	7
UCLA	2	6	1	2	4	1	2	6	1
UCSB	2	5	3	2	7	3	2	7	4
UCSC	1	4	0	1	4	0	1	4	0
UCSD	1	3	1	1	2	1	1	2	1
UT Austin	1	2	1	1	2	1	1	2	1
Wisconsin	1	1	0	1	1	0	1	1	0
Total	36	84	13	38	88	15	38	92	17



The Gigascale Silicon Research Center

<http://www.gigascale.org>

**“Empowering designers
to realize the potential of gigascale silicon by enabling
scaleable, heterogeneous, component-based design
with a
single-pass route to efficient
silicon implementation from a microarchitecture”**

Overarching GSRC Research Emphasis for 2001—... :

***“From Ad-Hoc System-on-a-Chip Design
to Disciplined, Platform-Based Design”***



The Gigascale Silicon Research Center

<http://www.gigascale.org>

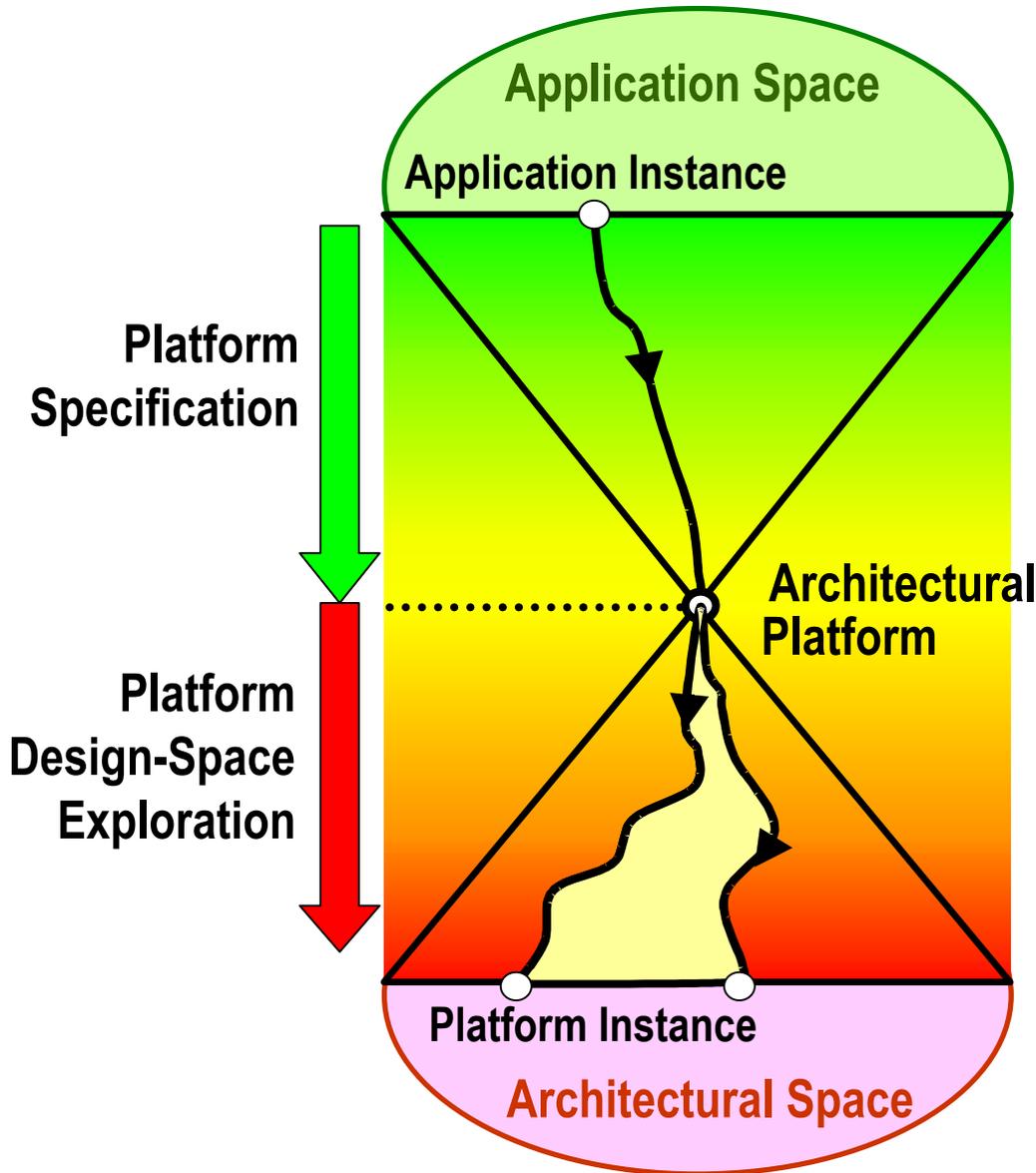
**“Empowering designers
to move from ad-hoc system-on-a-chip design
to disciplined, platform-based design by enabling
scaleable, heterogeneous, component-based design
with a
single-pass route to efficient
silicon implementation from a microarchitecture”**

What is a Platform?

- ◆ Broadly stated, platform is a **restriction on the space of possible implementation choices**, providing a **well-defined abstraction of the underlying technology** for the application developer
- ◆ New platforms will be defined at the **architecture-microarchitecture boundary**
- ◆ They will be **heterogeneous and component-based**, and will provide a **range of choices from structured-custom to fully programmable implementations**

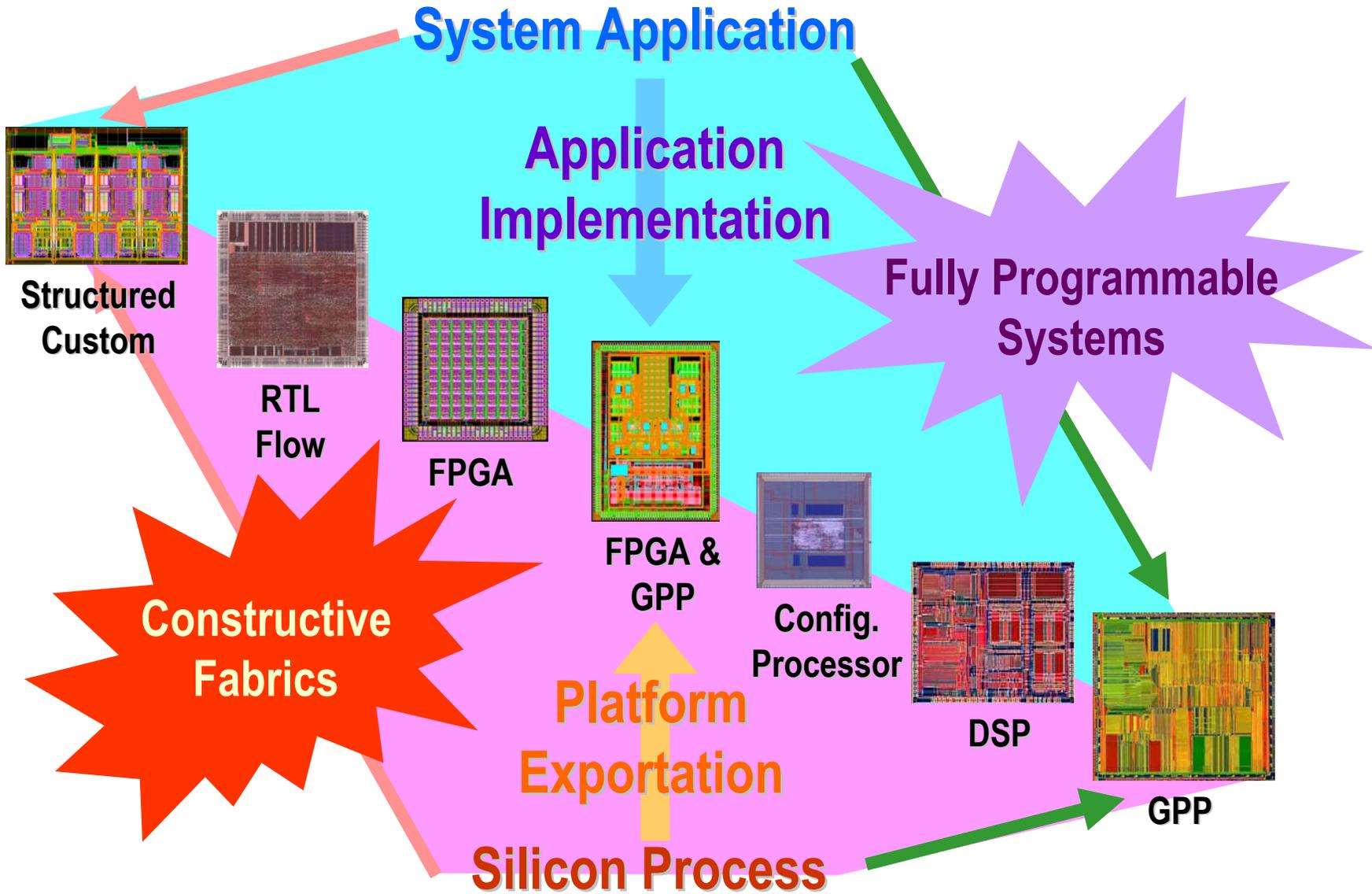
“Only the consumer gets freedom of choice;
designers need freedom *from* choice”
(Orfali, et al, 1996, p.522)

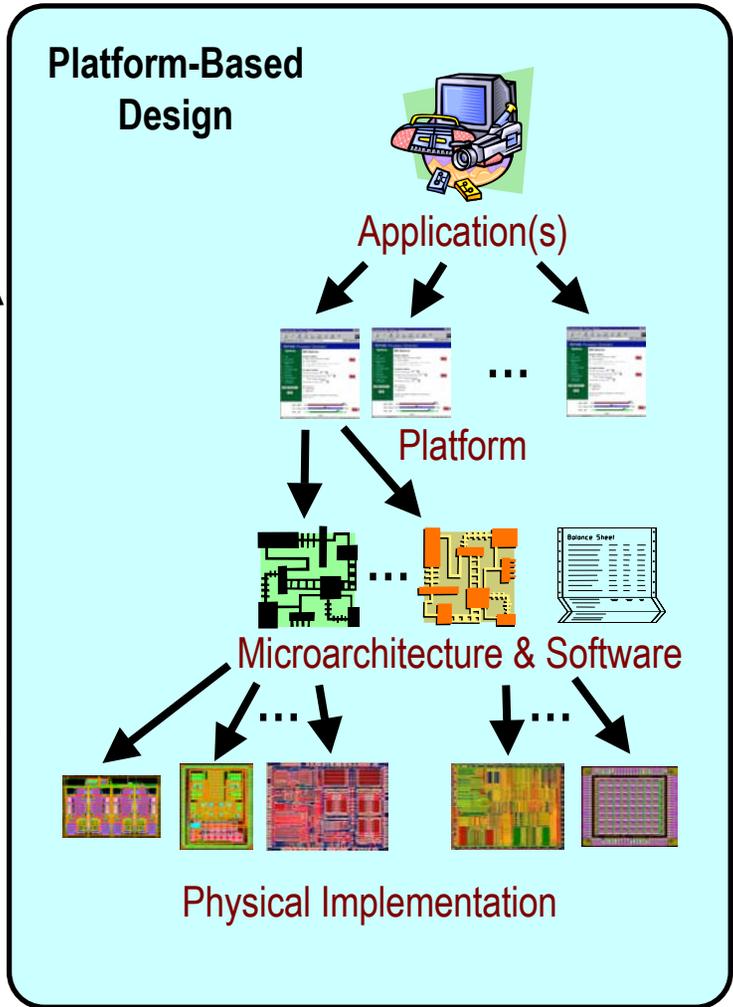
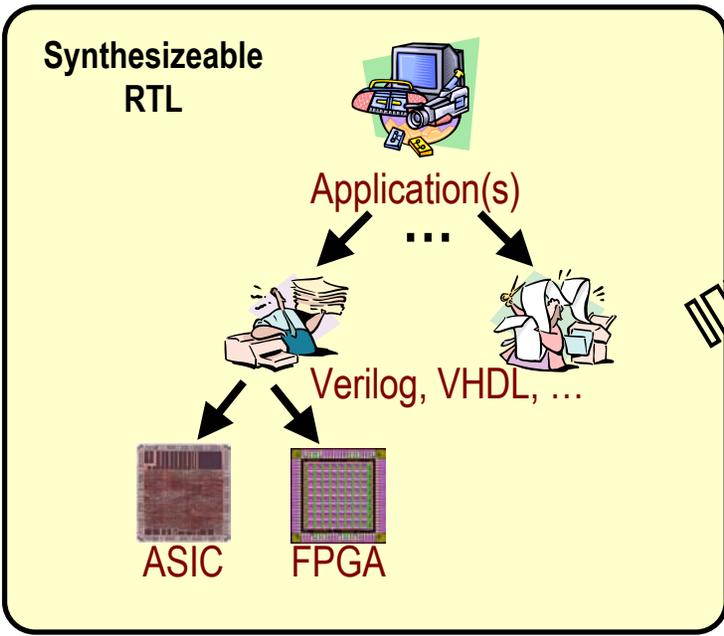
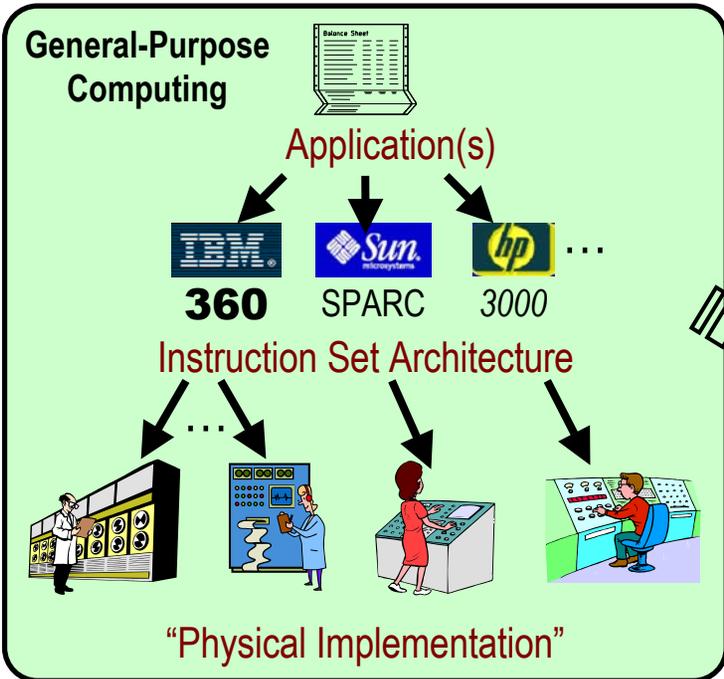
Platform Exploration



- ◆ **Common approaches:**
 - ◆ **Application-driven exploration of micro-architectures**
 - ◆ **Automated compilation into architectures**

Disciplined, Platform-Based Approach





Current Scenario – ASIPS on the Rise in Networking

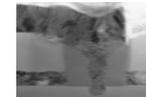
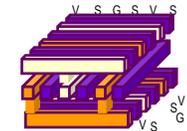
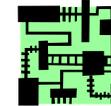
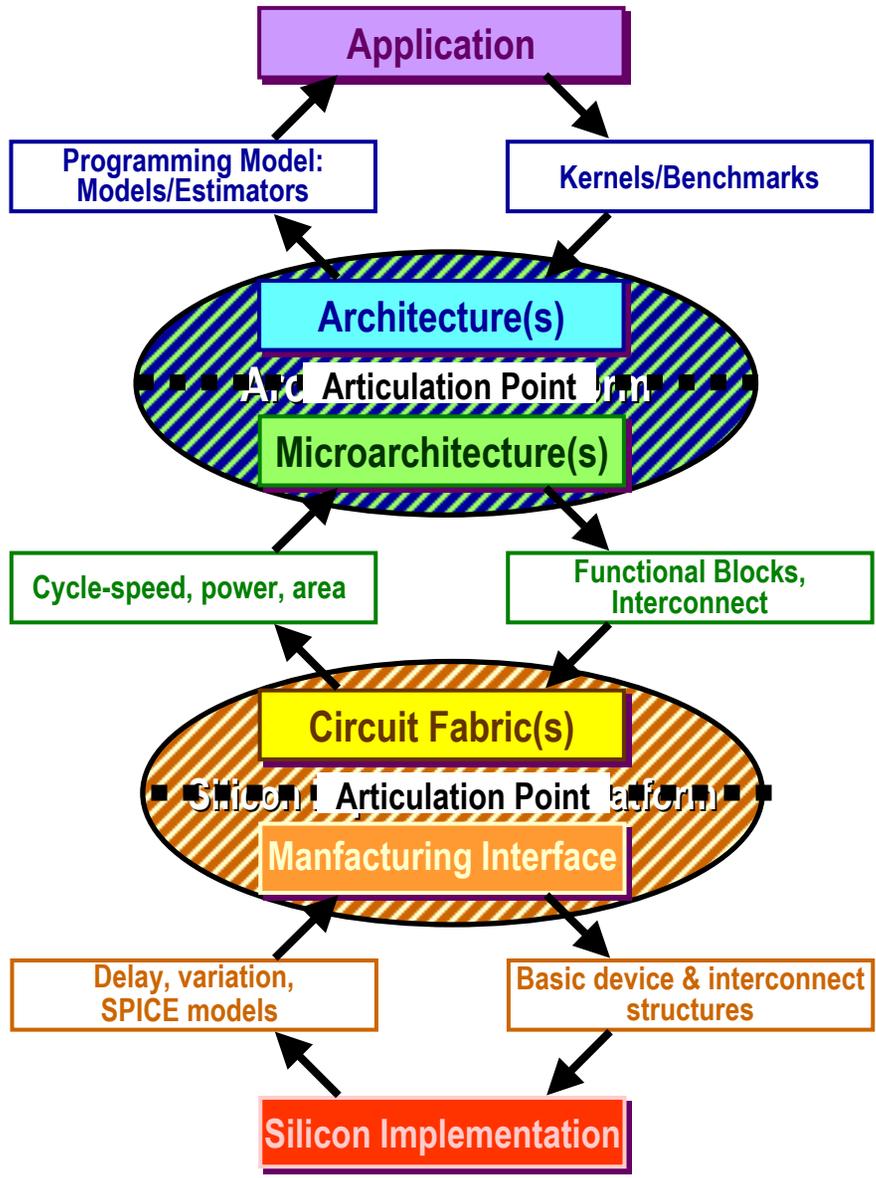
Company	Product	RISC based	Task Specific Processor based	ASIC
Level One	<i>IXP1200</i>	✓		
IBM	<i>PNP</i>	✓		
MMC	<i>nP</i>	✓		
Maker	<i>MXT</i>	✓		
Sitera	<i>PRISM IQ1200</i>	✓		
EZChip	<i>NP-1</i>	✓		
C-Port	<i>C-5 DCP</i>	✓		
Agere	<i>PayloadPlus</i>		✓	
Fast-chip	<i>PolicyEdge</i>		✓	
Hi-fn	<i>7711, 7751</i>		✓	
Xaqti	<i>TeraPower-CL</i>		✓	
Broadcom	<i>StrataSwitch</i>		✓	
Solidum	<i>PAX.port 1100</i>		✓	
Netlogic	<i>Policy, CIDR</i>		✓	
Switchcore	<i>CXE</i>		✓	
Entridia	<i>Opera</i>			✓

Source: GSRC MESCAL Group

Overarching GSRC Principles: June 2001

- ◆ **Orthogonalization of concerns**
- ◆ **Communication as first-class citizen**
- ◆ **Concurrency expressed at all levels**
- ◆ **Verifiable Assembly of Components**
- ◆ **Creation of Platforms for Self-Test**
- ◆ **Single-pass route to efficient silicon implementation from a microarchitecture**
- ◆ **Manufacturing faults must be identifiable and correctable**
- ◆ **Cost is a major driver at all levels**

A Discipline of Platform-Based Design



Distilled Principles on Platform-Based Design Derived from Breakout Sessions on June 17, 2001



◆ Application Development:

- ◆ **Spec should be verifiable, analyzable, simulateable**
- ◆ **Spec should use formal models of concurrency**
- ◆ **Spec should be easily expressed and the flexibility of expression should allow for exposing underlying concurrency**
- ◆ **Spec should capture function, constraints, and parameters**
- ◆ **Spec should capture functionality and constraints in an orthogonal form to implementation**
- ◆ **Computation and communication should also be orthogonal**
- ◆ **Environment should enable refinement process based on constraints and visibility of underlying cost functions**
- ◆ **Refinement process should itself be formal**
- ◆ **Refinement process should propagate constraints**
- ◆ **Environment should enable design re-use including legacy issues**
- ◆ **Environment should enable fast, efficient, and robust design re-use (as an assembly of encapsulated components; as the incremental evolution of existing designs)**
- ◆ **Specification must be in form that is verifiable/analyzable/simulatable.**

Distilled Principles on Platform-Based Design Derived from Breakout Sessions on June 17, 2001



◆ Application Implementation:

- ◆ Environment should enable mapping the concurrency of the application to the concurrency of the architectural platform
- ◆ Environment should enable refinement process based on constraints and visibility of underlying cost functions
- ◆ Environment should provide the ability to do educated trade-offs in a comprehensive design-space exploration
- ◆ Environment should enable the designer to redictably / reliably realize an implementation within constraints through constructive estimation / quick path implementation
- ◆ A correct-by-construction methodology is the **ONLY** way to solve the verification problems
- ◆ Environment should allow for incremental changes in either functionality or constraints either from above (application requirements) or below (platform changes) to be rapidly accommodated.
- ◆ Environment needs to maintain consistency with specification (downward by synthesis and/or upward by verification).
- ◆ Robustness (fault tolerance) is necessary even when design "correct by construction"

Distilled Principles on Platform-Based Design Derived from Breakout Sessions on June 17, 2001



◆ Architecture Platform Development:

- ◆ **Driven by set of application benchmarks and application drivers**
- ◆ **Based on metrics and models that can be exported to application development**
- ◆ **Development is based on components that are robust, verifiable, and allow plug & play methodologies**
- ◆ **Architecture, simulator, compiler, (IDE) are developed concurrently using a single consistent verifiable data model with multiple views**
- ◆ **This environment enables concurrent optimization of hardware/software**
- ◆ **Involves a comprehensive, educated, design space exploration matched to concurrent structure of application domain**
- ◆ **Exports an architectural platform programming model to enable platform (re)-use**
- ◆ **Restricted set of components enables verifiable assembly and mapping**
- ◆ **Must verify across cores, peripherals, busses, and software in way that can reuse verification.**
- ◆ **Determine methodologies that support the development of appropriate programmer's models for conventional and unconventional architectures**
- ◆ **Environment Enables application-specific performance optimization**
- ◆ **Common, integrated, framework for exploring design space (power, delay, area, cost, . . .) (Digital, analog, RF, . . .)**
- ◆ **Platform necessarily lends to re-use (by classes of applications)**

Distilled Principles on Platform-Based Design Derived from Breakout Sessions on June 17, 2001



◆ Architecture Platform Implementation:

- ◆ Environment should enable an implementation sets that span the performance space adaptable to the environment (e.g., energy-efficient)
- ◆ Environment should enable an implementation that is robust, verifiable, and predictable
- ◆ Environment should enable an implementation that scales & ports across technologies
- ◆ Environment should enable design-space exploration through rapid implementation (constructive estimation)
- ◆ Implementation should be communication centric
- ◆ Environment should support RF and analog (e.g. sensors, actuators)
- ◆ Implementation should be robust under fault / process variations / implementation variations /operating conditions
- ◆ Design methodology & tools must be developed together

“Not Just Research As Usual”

- ◆ The GSRC is a **unique experiment** in long-range, collaborative research, enabling **broad collaboration** across many areas of EDA and Design
- ◆ In the **1960-1980’s DARPA** played a **key role** in creating and maintaining a collaborative community in design and architecture
 - ◆ Xerox PARC & the Alto, Berkeley Unix, RISC, RAID, Integrated EDA Systems...
- ◆ GSRC is about **rebuilding and maintaining such a community** of researchers in many fields related to **silicon design productivity**
 - ◆ By **leveraging modern, distributed collaborative infrastructure**
 - ◆ By enabling and supporting a series of research **themes**
 - ◆ By developing and maintaining a well-defined, but broad goal—the **Moon Shot**—that serves to integrate all participants
- ◆ Thank you for your confidence and your ongoing support!