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It's a Small, Small World

The philosophy guiding MTO's investments is captured in our theme for today, "It's a Small, Small World"—a world in which we are working to shrink complex systems capabilities into chip-scale packages.

A world with a future that we believe lies in the integration of today's three core information age technologies: microelectronics, photonics, and micro-electro-mechanical systems or MEMSs. A future where heterogeneous integration of these technologies creates a new revolution in chip-scale capabilities for military information systems.

In general, I like to discuss our programs in the context of how advances in these three core technologies and the benefits obtained through their integration onto either a single chip or, more typically, combined to form a heterogeneous chip-scale, system-in-a-package. Because it's at the intersection of these technologies that we find some of the most interesting applications for DoD systems and the greatest challenges for technologists!

- Integration of MEMS with RF electronics and photonics
- Integration of photonics with digital and analog electronics and, in recognition that microelectronics is really two disciplines, digital and RF/analog
- Integration at their intersection, to create mixed signal circuits

Today, microelectronic chips and photonic and MEMS components are pervasive across military systems. They are key enablers for achieving the information superiority our forces currently enjoy, major contributors to establishing for our military forces the combat advantage derived from being able to see farther, with greater clarity and with the ability to communicate critical information in a timely manner. As we look to the future, our model is the spectacular success that monolithic integration of millions of transistors has had in reducing racks of equipment onto a single chip, so that after more than 40 years of research and development, today's electronic ICs are delivering complex, signal processing and analog/RF functions on a chip.

But as successful as this has been, the future lies in further increases in the level of integration to create even more complex capabilities. In particular, integration among the core technologies in a strategy to create truly world-class, chip-scale, microsystem capabilities with built-in digital processing and intelligent control for maintaining and extending defense information superiority.

Exploiting embedded intelligence to enable chips capable of providing:

- Sensor systems with enhanced RF bandwidth and multiwavelength optical sensing
- More versatile signal processors for extracting useful signals from background interference, noise, and jammers
- High-performance communications links delivering assured bandwidth on demand
- Intelligent, chip-scale microsystems that enable conversion of complex data into actionable information in near real-time

Taken together, our ability to enhance these capabilities at the chip level that translates into systems that will enable our forces to think and react faster than the enemy, that extends information superiority through

innovation of new and enhanced hardware for collecting, processing, and managing information flow within and among systems.

Consider a generic information system representative of a typical military platform. It is comprised of a sense suite, largely analog and operating anywhere from RF to the ultraviolet and including mechanical and bio sensing; a signal processing suite, largely digital and with the broadband interconnection capacity required for rapid data exchange among platform subsystems; and with the embedded controllers that can reach out to manage all the subsystem operations. And finally, an actuation suite, which is typically analog in nature, but in our model also includes off-platform data comm links as well.

I have in mind that such a platform could be an individual warfighter with wearable sensors and computers, in which case we're truly talking about a small, small, chip-scale world; a manned or unmanned air or ground vehicle where the quest for reduced size, weight, and power, with increased functionality, drives chip-scale solutions; a complex AWACS or SIGINT platform or a city-size vessel where increased stand-off distances, and the greater complexity of the systems we want to implement, drive us to chip-scale integration of basic functions; or the entire active theater of operation where the challenge is to create components that enable truly network centric operations.

Regardless of the platform's physical size, information generation and flow relies on a distinct network of subsystems for sensing, processing, communicating, and acting on data generated and collected over a wide spectral range. Data captured in analog format by sensors designed to obtain as accurate a representation of what they sense as possible. Data that when transferred to processors can be transformed into actionable information. The value of this data, the information derived from it, and the decisions that flow from this information are only as good as the resources available to carry out these sense and processing functions. And it is these resources that are critical to translating the reality of the battle theater into the cyberspace of decision-making and action initiation.

This collection of sensors, processors, and links making up a military information platform create a complex system that must operate under conditions seldom encountered in commercial world applications. An emerging issue is the fact that, in normal operation, today's sensor platforms are capable of generating much more data than is actually required. Creating a major challenge in how to intelligently manage the collection to focus primarily on what is really useful. We believe this challenge can be met, in part, by incorporating greater levels of signal processing and intelligent control within the sensor elements creating embedded intelligence that ensures the data passed along for top-level analysis and consideration is only what is really relevant.

In keeping with today's theme, MTO is focused on innovation within the three core information technologies to exploit their most advanced capabilities in creating compact, small-small, chip-scale packages for ubiquitous application across the battle space. Because it is only through continued innovation, and the expanded application of microsystems, that the DoD can truly maintain information superiority.

Now, I'd like to spend a few minutes highlighting some major MTO program directions that support the vision I've just outlined. Beginning with our microelectronic programs.

Chip-scale microelectronics is the core enabling technology for military information systems. DoD and DARPA have a long history of investments in this technology. When measured by the two simple metrics, circuit speed and transistor count, we can view progress in microelectronics over the last 25 to 30 years as advancement along two parallel, related, but independent, tracks and the challenges this advancement has created.

The first tracks advances in silicon CMOS digital circuits. In terms of speed, CMOS is not considered a high-performance technology. Instead, tracking Moore's Law, as the number of transistors per square centimeter increased, and our ability to exploit these increases to create complex signal processing chips, the challenge has been dealing with the complexity of chip architecture and design. In response to this challenge, a remarkable set of computer-aided design, or CAD, tools have been developed to enable us to cope with this complexity, so that today we have the ability to design extremely complex chips containing

millions of transistors. In fact, the Semiconductor Industry Association has developed an approach to road-mapping the challenges to sustaining Moore's Law. Over the past 2 decades, the lithography and materials/material-processing research communities have successfully maintained a steady stream of advances along this roadmap, permitting the continued scaling of CMOS devices to smaller and smaller dimensions.

At DARPA, our programs historically have supported these advances, but in recent years, we have looked beyond the road-mapping process. For example, only a few years ago, modeling predicted that scaling CMOS devices below 70 nm would not be possible. But a little more than 2 years ago, in our Advanced Microelectronics Program, we demonstrated devices with excellent transistor characteristics having critical dimensions down to 20 nm. At these dimensions, we believe we have truly reached the logical conclusion of the advances in transistor density enabled by scaled silicon.

Today, our pioneering results have been confirmed across the industry. Based on current Moore's Law predictions, ICs incorporating transistors with these critical dimensions, assuming they are truly manufacturable, will not be available commercially until a decade from now. But, with the industry passing through the 100 nm generation, with preliminary results being reported for 90 nm devices, and with many problems remaining to be addressed, we have a clear vision to future designs containing trillions of nano-scale CMOS transistors.

As exciting as the challenge of implementing chips with trillions of transistors is, what I believe is truly remarkable about these deeply scaled devices, particularly from a DoD perspective, is that they exhibit pico-second switching speeds, speeds that correspond to tera-hertz bandwidth capabilities. With pico-second switching speeds, we see the potential for applications beyond smaller IC dimensions and anticipate a complementary revolution in silicon, a revolution exploiting the speed of nano-scale CMOS leading to high-speed circuits for applications extending from the commercial world's interest in wireless systems-on-a-chip to a host of new military-specific applications integrating unique RF circuit and high-speed signal processors that will enable DSP control algorithms designed to operate with greater than 20–30 GHz clock frequencies.

As we enter the small-small world of nano-CMOS electronics, the challenges really lie on two fronts: First, what complex DSP applications, realized with chips containing over a trillion transistors, can the military take full advantage of? And, second, how can we fully exploit CMOS chips capable of operating at multiple gigahertz speeds in military RF systems? We'll have more to say on these points later.

On the second evolutionary track, which until recently in the United States was driven primarily by military applications, we have invested heavily in compound, semiconductor-based technologies for high-performance, high-frequency, monolithically integrated, microwave-ICs and companion technologies for advanced signal processing mixed analog/digital circuits. The impact of these programs is evident in both their widespread incorporation into military RF systems and the role the Defense contractor community has played in delivering MIMIC technologies to the commercial wireless world.

The challenges on this track have been different from those of CMOS circuits. The MIMIC challenge has been and remains threefold:

- Achieving a high degree of precision in the control of the material structures that comprise individual transistors to achieve a uniformity of response across the wafer unheralded in digital applications
- Incorporating on-chip bulky, passive, impedance-matching elements
- Managing interconnections to control impedance levels for signal propagation across chips

These added burdens in design, combined with the limited production of MIMIC chips and the lack of common core circuit designs, mean that we have yet to see the level of CAD tool development to serve this community that is available for digital designs. Even given the superb control we have over material deposition, we have not really evolved the control over processing to the degree that silicon producers have

achieved, with the result that today's leading edge, mixed-signal, compound semiconductor-based RF/analog chips are limited to only a few thousand transistors per circuit.

As we move to more complex chip-scale RF systems, a substantial improvement in our ability to design and fabricate more complex chips would enhance greatly the capabilities of military RF systems. It is with all these experiences in mind that we have created a number of new initiatives for MTO's microelectronics programs.

First, since detailed analysis indicates we really are hitting hard physical limits as quantum scale effects begin to dominate performance of deeply scaled classic MOS devices, we are forced to look beyond traditional approaches to find alternative technologies that will allow extending operation to even smaller dimensions. In this endeavor, we are truly at the threshold for defining a new meaning for electronics of a small, small world. With the microworld that we have been laboring in for so long giving way to the exotic, quantum-mechanics dominated, nanoworld of the future.

To investigate what lies ahead, DARPA is exploring this new world in a multi-office initiative titled "Beyond Scaled-Silicon CMOS." Among the programs underway are:

- MTO's molecular electronics, or Moletronics Program, which we'll hear more about later
- DSO's spin-based electronics programs
- Joint DSO/IPTO quantum information and science technology, or QuIST Program
- IPTO's Biocomputing Program.

Major strides are being made in all these domains, and I'll leave it to the other office directors to tell you about their specific programs.

However, I take pride in the fact that it was largely the successes to date in our Moletronics Program that was responsible for the selection of nano-electronics as the "Technology of the Year" by the journal *Science* in its December 2001 issue. And now MTO is preparing to address the next molecular electronics challenge, the challenge of exploiting these preliminary results to create large-scale circuits and to interface these nanoscale molecular devices to traditional silicon CMOS circuits, so we can begin to answer the question, "Where do I plug my keyboard into my molecular computer?"

The second initiative deals with how we can exploit the increasing signal processing capabilities enabled by deeply scaled CMOS, beginning with current generations of 100 nm CMOS and SiGe extending over the next decade as we shrink critical dimensions to 10 nm. To scope out the possibilities, we launched a couple of studies over the last 2 years, including a major one aimed at the architecture of microprocessors at the end of Moore's Law that we titled, "The Last Classical Computer." This study was carried out by the Information Science and Technology Study Group. Our program managers created the initial working title, but the ISAT academics quickly renamed the study "The Next Classical Computer" because, in the end, what they found themselves engaged in was investigating the new architectural challenges and capabilities that deeply scaled CMOS offers. But regardless of what you call it, the study outcome identified two compelling trends that I believe will really revolutionize digital signal processing.

The first trend is driven by the recognition that, as clock frequencies continue to increase, it will take many clock cycles for signals to propagate across a chip. One result is that current signal processors, based on Von Neumann architectures, are becoming less and less efficient in their utilization of the inherent switching speed of individual gates. The study suggests that, by the end of the decade, there likely will be more than four orders of magnitude difference between the processing capacity of chips based on current designs and what could be achieved with chips based on new architectures that can fully exploit the discrete device capabilities.

Without going into the details, the challenge is that we need to transform from computation-intensive, serial-processing designs to more parallel, communication-intensive designs. We will need to architect and implement chips that incorporate the equivalent of a chip-scale local area network or "nano-area" network with data flow and management across the chip handled in somewhat the way today's networked

workstations operate. The new design paradigms will be based on how best to really exploit this transformation. The payoff will be chips with near-human-like cognitive abilities.

The second trend is driven by our recognition that as we increase the clock speed of digital chips into the tens of gigahertz range, we are creating the possibility for incorporating a significant level of real-time digital control and intelligence into RF and analog mixed signal circuits. We're not alone in recognizing these capabilities, witness developments in commercial wireless appliances. However, these commercial applications are just the tip of the iceberg for what combining chip-scale digital intelligence and high-speed, mixed-signal, and RF can achieve through monitoring and controlling performance in real-time for future military systems applications.

For example, we ask the question, "What can a 30-GHz processor achieve in monitoring performance and controlling in real-time RF MIMICs operating at a fraction of this speed?" To begin with by using the processor to control electrically tunable passive elements, we can optimize chip performance in real-time as the input signal is swept over a broad frequency range. At the most simple level, intelligent control of MIMICs will enable adaptation of passive circuit elements, after manufacture, to overcome limitations of processing and greatly improve the yield of useable parts.

In effect, every chip will come with an RF designer built in, enabling chips that can adapt their performance to the characteristics of the actual manufactured transistors rather than on the basis of model devices. In other words, they will be able to think and self-adapt in real-time in response to changing environments and in support of demanding applications.

Significant challenges exist in advancing the hardware that will be required in the search for the right mix of silicon and III-V as we attempt to marry the intelligence of fragile, nanoscale, gigaspeed silicon chips with the heavy-lifting capability of traditional, compound semiconductor MIMIC technologies. Additional research is required to determine the right architecture and control algorithms to realize the full potential of these new capabilities. The exploration of this new nano-electronics domain will require the resources of both the MTO with its hardware focus and the newly refocused IPTO with its architecture and control algorithm focus.

We identify this new initiative as the development of intelligent microsystems technology. Specific programs beginning to address these ideas include MTO's Technology for Efficient Agile Microelectronics (TEAM) Program, which is largely focused on addressing what can be done with silicon, and our Intelligent RF Front-Ends Program, which is concentrated on developing RF MIMICs that incorporate adaptive controls. Some ongoing programs that also address these issues include our NEOCAD Program, developing design tools for mixed signal circuits; IPTO's Polymorphous Computing Program; and TTO's mission-specific processors. Additional programs are planned.

Finally, within our microelectronics portfolio, we continue to explore new ways to enhance the performance of traditional semiconductor electronics. In this respect, we're currently pursuing a number of options.

First, recent advances in materials capabilities have pumped new life into the promise of the wide bandgap semiconducting materials silicon carbide and gallium nitride. These materials have been of interest for high-power RF and DC/quasistatic, high-power, switching applications for some time. With bandgap energies greater than 3eV and thermal conductivity and electron mobility significantly superior to competitive materials, their intrinsic properties make them attractive candidates for these applications. But, the flip side of their wide bandgap energy is the extreme difficulty to prepare high-quality starting material for fabrication of devices.

The prospects for these materials recently have changed dramatically. Significant investment in materials research has been stimulated in large part by applications to light-emitting diodes operating in the near-ultraviolet and blue-green regions of the spectrum. With this reawakened interest in silicon carbide and gallium nitride, promising small-scale research demonstrations of prototype RF and high-voltage transistors have occurred.

Substantial hurdles remain in terms of defect reduction and controlling the deposition of high-quality epitaxial material to enable capability comparable with what we can not achieve with GaAs and InP. We are beginning to address the critical issues limiting the practical application of these materials in two new programs: high-frequency and high-power wide bandgap semiconductor technology. We're working closely with the Service S&T organizations to ensure rapid transition of the results of these program to the ultimate end users. In addition, building off the commercial world's interest in gallium nitride materials for light-emitting diodes operating in the visible region of the spectrum, we have initiated a program to develop extremely short-wave uv sources based on gallium aluminum nitride to address DoD needs in biological threat detection.

A second option we are pursuing is testing the limits of very high-frequency performance of III-V semiconductor electronics. In the first of two programs we have launched, the Antimony Based Compound Semiconductor (or ABCS) Program, we're focused on the utility of low bandgap energy materials based on antimony compounds for extremely high speed and at low power. One promise here is that through the use of resonant tunneling devices—in conjunction with the low-power switching characteristics of these devices—very high-speed ICs can be realized. Our goal is to demonstrate circuits operating at very high frequency—frequencies greater than 100 GHz—operating at extremely low power of less than 1 femto-joule per operation and with integration levels of at least a few thousand devices. With these materials, there is again an opportunity for photonic device applications.

In a new program, Technology for Frequency Agile Digitally Synthesized Transmitters (or T-FAST), we are building on the already proven capabilities of indium phosphide materials. Currently, InP processing technologies limit us to ICs with no more than a few thousand transistors and, unlike comparable silicon based ICs, these limitations require us to scale back operation in high transistor count circuits to clock frequencies more than an order of magnitude below the peak cut-off frequencies of discrete transistors.

The approach we'll take is to develop new fabrication processes designed to squeeze the maximum performance from each device even when embedded in a dense IC. We will do this in a way that will allow extending the high-frequency performance of individual transistors, while also enabling a substantial increase in circuit density and clock speed. The goal will be to demonstrate substantial increases in the number of transistors, to the level of 10 to 100,000 devices per circuit, that will allow more complex high-speed signal-processing applications, with operating clock speeds up to 100 GHz. We fully anticipate that success in this effort will revolutionize mixed signal technologies for future multifunctional RF systems.

Now I'd like to briefly comment on our micro-electro-mechanical systems programs.

MEMS development over the past decade represents another continuing MTO investment success story. In 1992, there was little industry involvement and virtually no fabrication infrastructure anywhere in the world. Since that time, DARPA's significant investments have yielded revolutionary capabilities ranging from commercial applications in projection display technology and inertial sensing, to meeting unique military needs in monitoring the readiness of missiles and projectiles, and RF MEMS switching components having very low insertion loss compared to alternative switch technologies, which are now emerging from the laboratory. Additional MEMS applications we're developing include:

- Multi-axis micromirrors for replacing bulky gimbaled optics to provide precise three-dimensional positioning for agile, free-space, optical beam steering and control
- MEMS-enabled chip scale biosystems that mix complex on-chip fluid and mechanical components for chip-scale chemical processing
- MEMS-inspired processing to create sensor elements for uncooled IR detector arrays to achieve high resolution with very small bolometers having precision thermal management for efficient, sensitive, IR sensing
- Power generation on the microscale, compatible with powering MEMS remote sensors.

But what, in many ways, is even more exciting is the promise of MEMS resonators with nanoscale dimensions. With these resonators, we are achieving a very high-frequency response that is enabling new applications for MEMS in RF filtering and signal processing. In a new program, we are locking these resonators to atomic transitions to create radically new designs for stable RF source. Our goal is to realize atomic clock timing precision on a chip. Success in this area will revolutionize the way timing is dealt with in systems while obviating the current dependence on GPS signals for many critical applications.

Professor Clark Nyugen from the University of Michigan recently joined us and will lead the MEMS Program in MTO. He will discuss our MEMS Program in more detail in a few minutes.

Now, I'd like to turn to the third core MTO technology, the application of photonics in military information systems. For some time, our photonics programs have been focused on two areas with some spectacular successes: photonic sensors and photonic interconnections in high- performance systems. But rather than going into any detail, I'd like to introduce Dave Honey, who for the time being is, in addition to being MTO's Deputy Director, is managing our office's photonics portfolio.

And as I turn the podium over to Dave, I'd like to thank you for your attention and outline the remainder of MTO's presentations. Following Dave, we'll hear from four MTO program managers who will provide additional details on specific programs. First, Clark Nyugen will review MEMS technology, and then John Carrano will discuss his Steered Agile Beams Program. John will be followed by Edgar Martinez, who will provide greater details on how we're transforming microelectronicis. And finally, Kwan Kwok will wrap up with a review of one of our most forward looking efforts, the Moletroncis Program.